

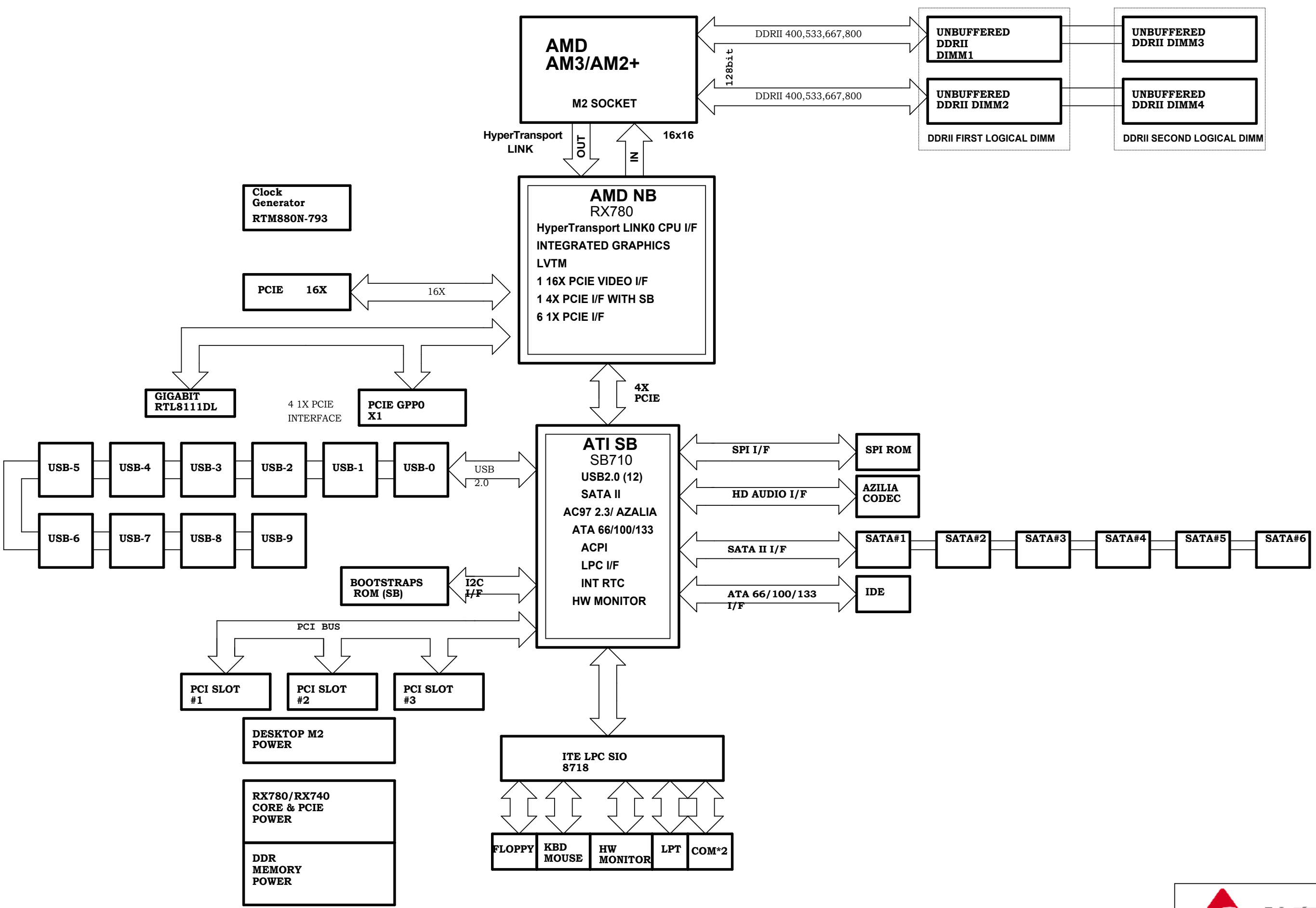
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45	BOM

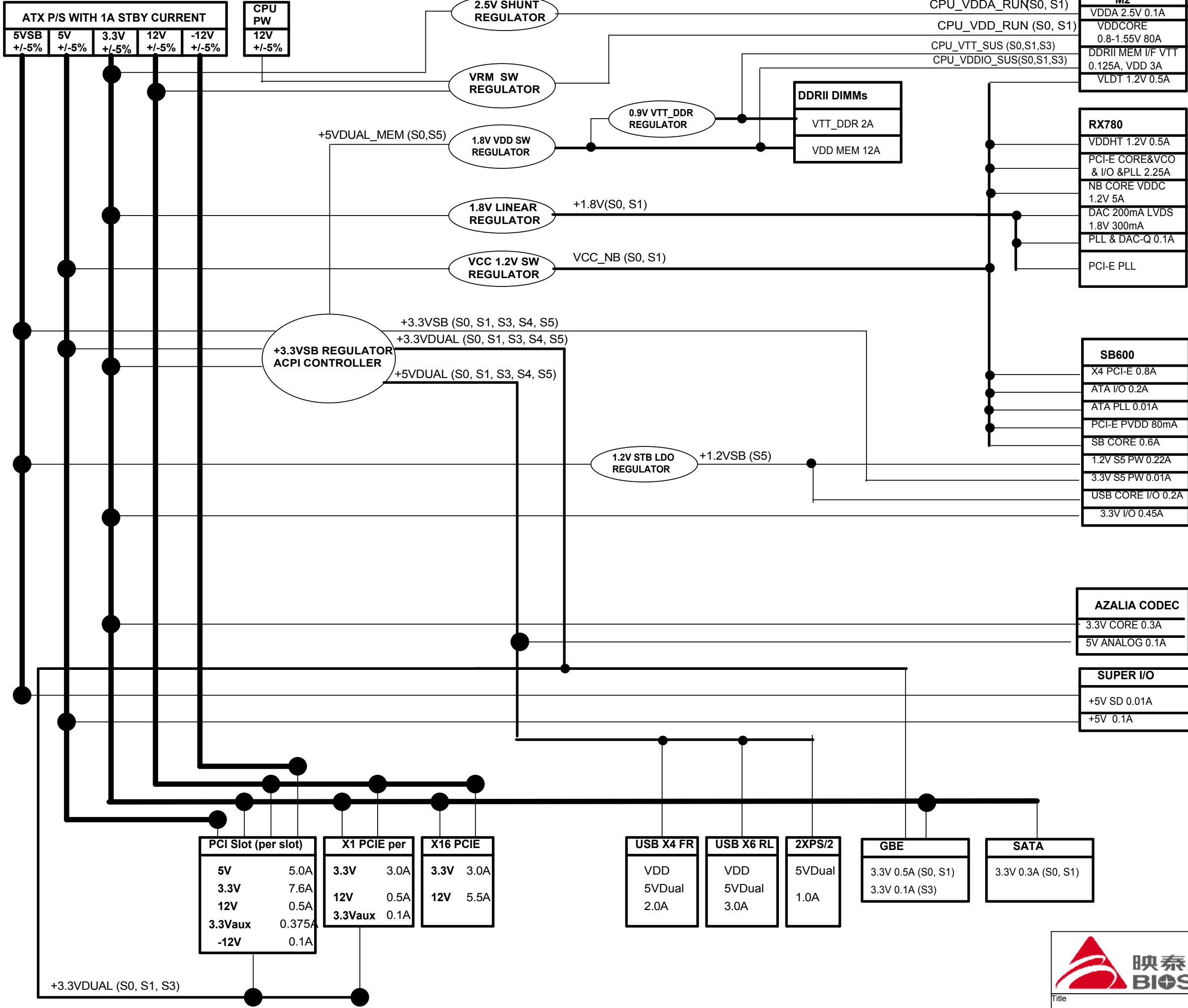
A78XC-A2S (RX780&SB710)

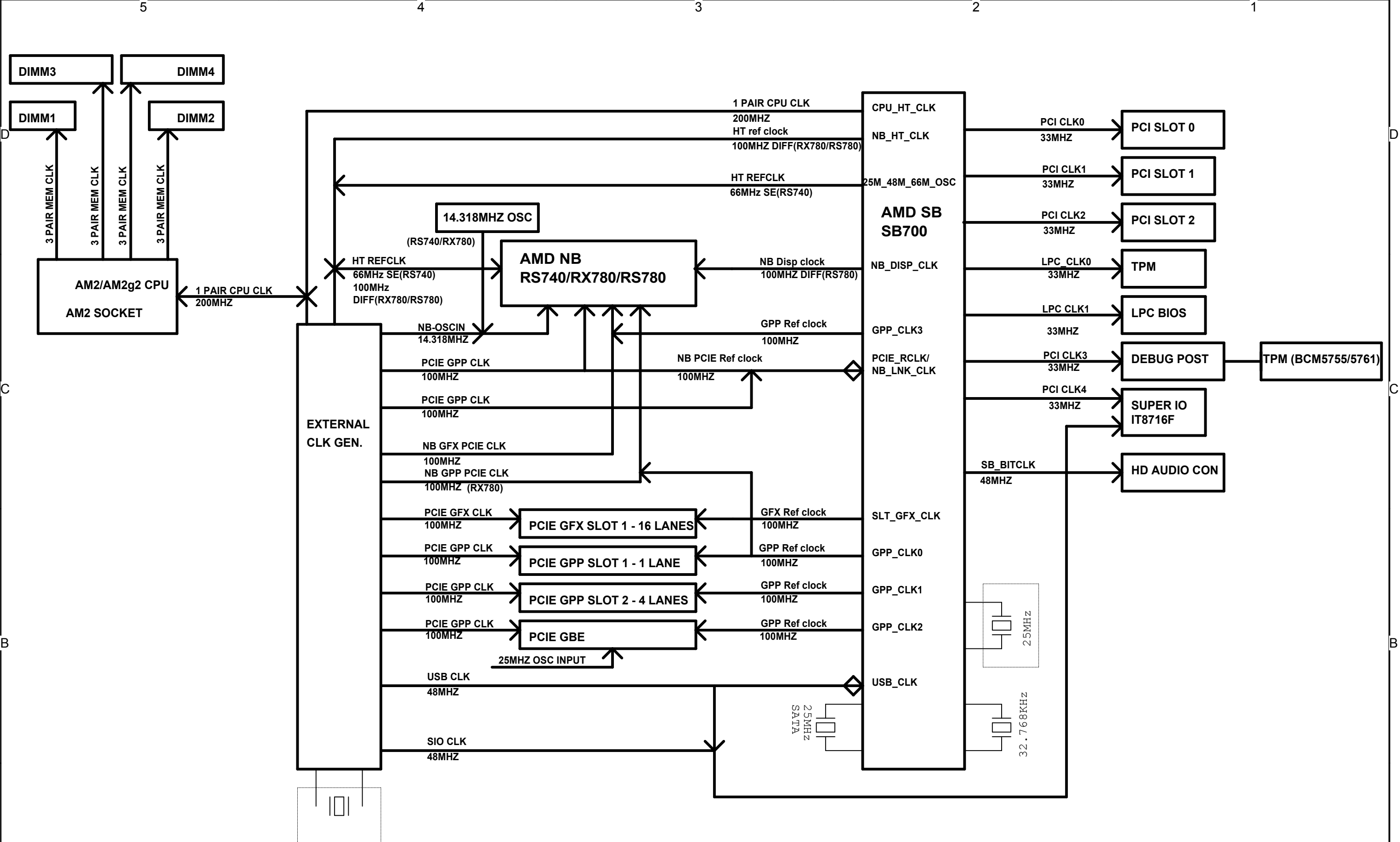
Marketing Name : A770E

REV:6.3

DDR2 X 4 Dual channel , PCI-Ex16 X 1 , PCI-Ex1 X 2 , PCI X 3 , RTL8111DL PCI-E Lan , AMD K8-940







1. 2009/07/13  
Change All SMD 0603 RC To 0402  
Change DDR & NB PWM VIN DIP CAP To " 560UF-S 6.3V 8X8"  
Exchange JUSBV1,JUSBV2 Silkscreen  
Move CT15 Far away SYS\_FAN1


2. 2009/07/14  
Update SIO Page: LAN\_RST# & PCIEX16\_RST#  
Add ACC Function

3. 2009/07/15  
CPU PWM ST 6717 改成ISL6323B  
Add SPI ROM WP# Function

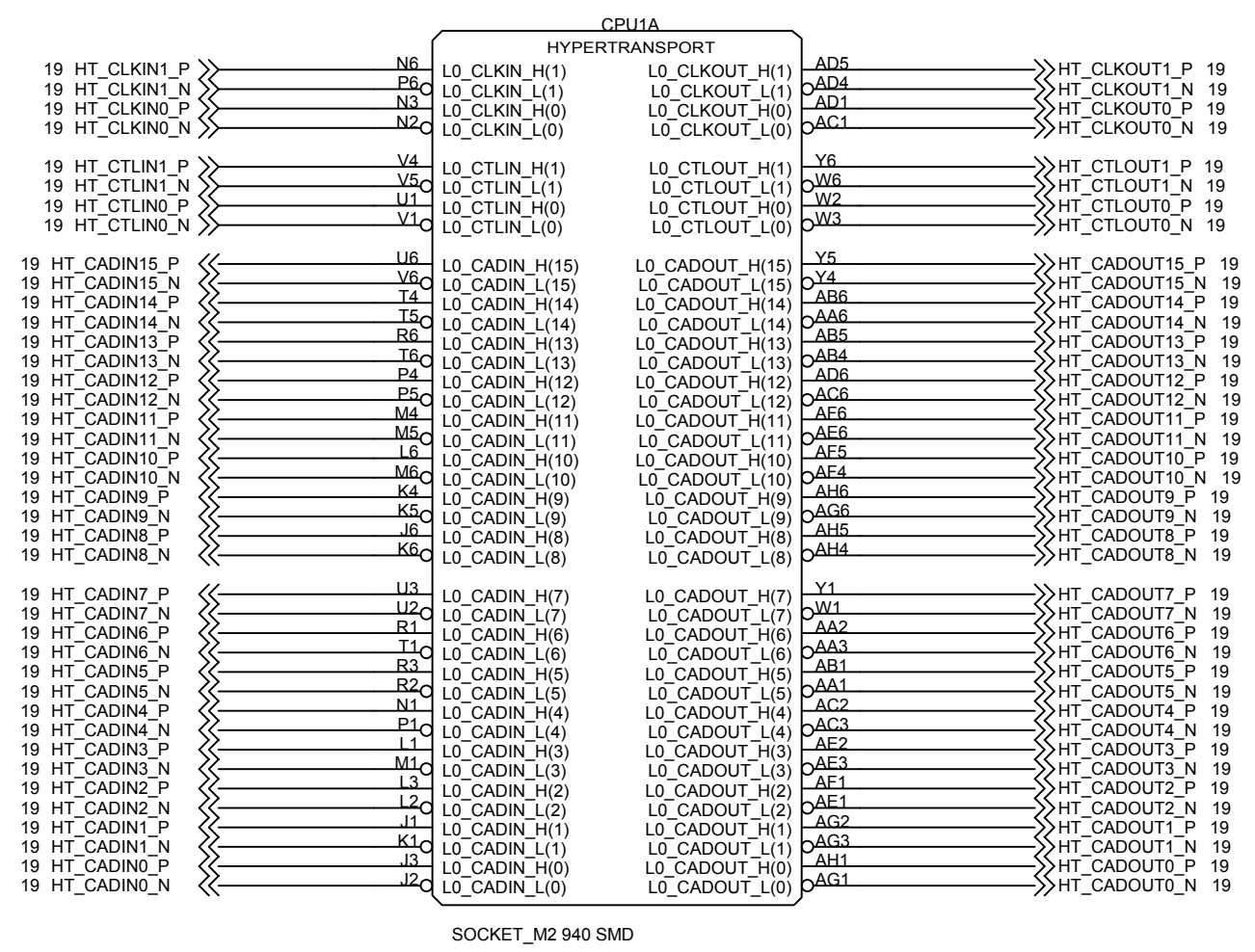
4. 2009/07/22  
CPU PWM Page: NI PSI Block  
Board ID Change From GP35,GP36--->GP59,GP60

5. 2009/07/23  
Board ID Change From GP59,GP60--->GP35,GP36,Don't Change it  
CPU PWM Page: PR40 715 1%-->1.33K 1%; PR64 0 /NI-->42.2k 1%;  
Low Side Left MOS SMD Solder PAD Reserved

6. 2009/07/27  
Change Audio Layout SPEC: L R Signals Always Routing Together  
Change Audio Jack To GND\_AUD

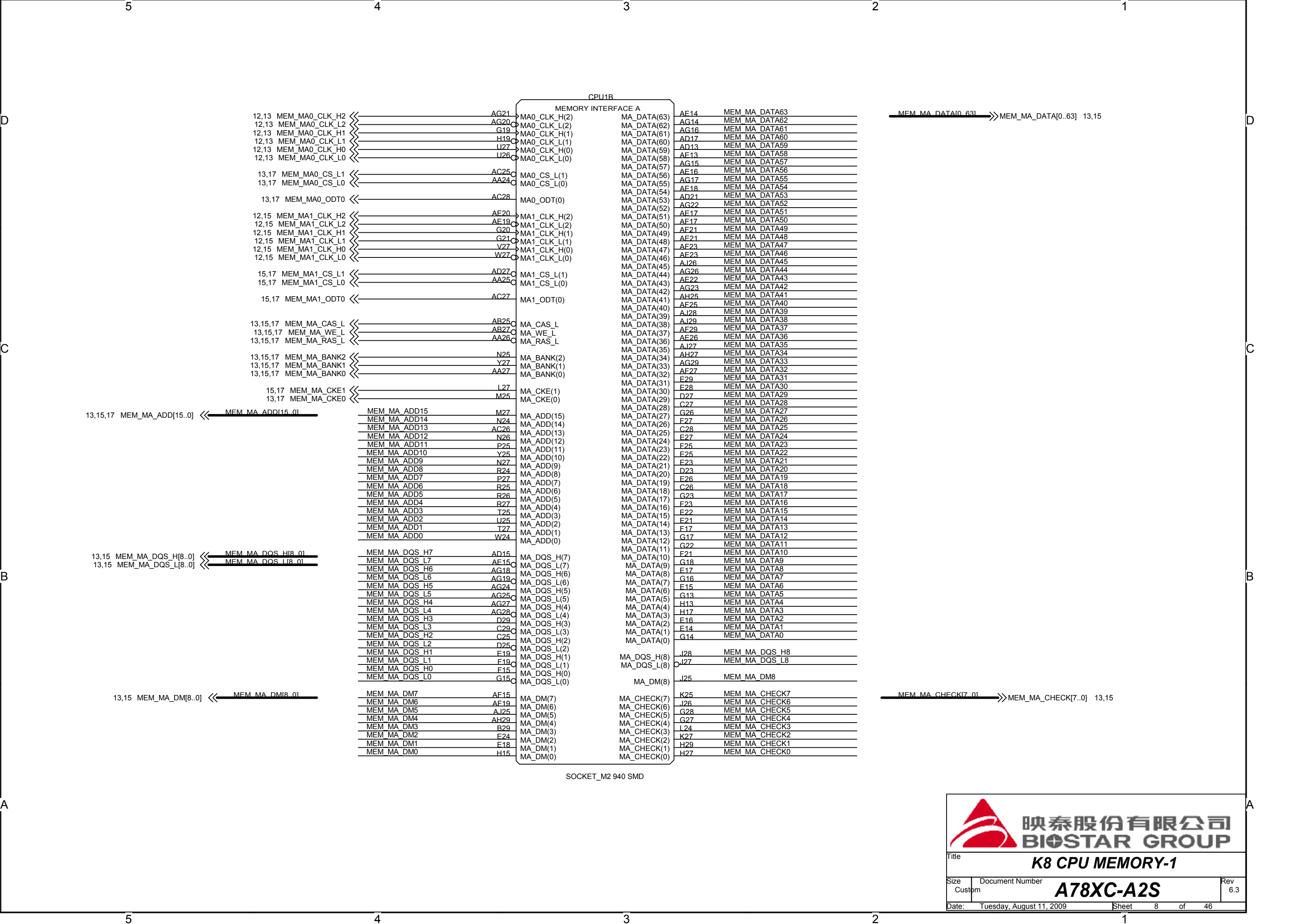
		
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Size Custom	Document Number <b>A78XC-A2S</b>	Rev 6.3
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HyperTransport

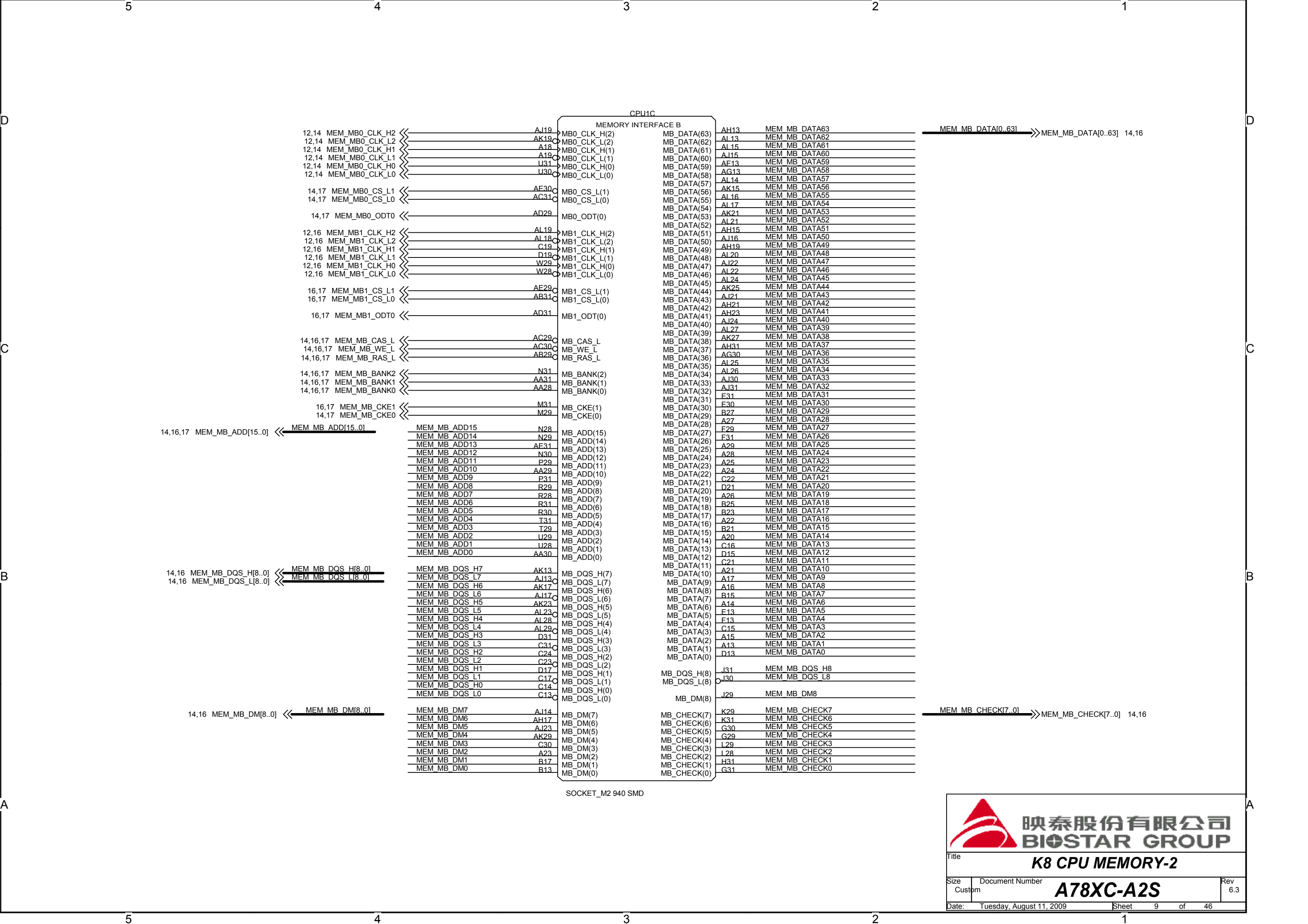














5

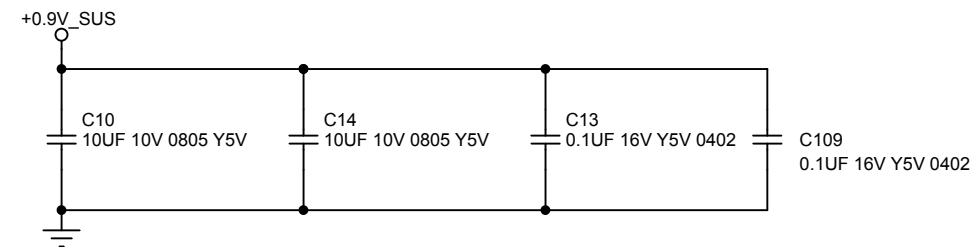
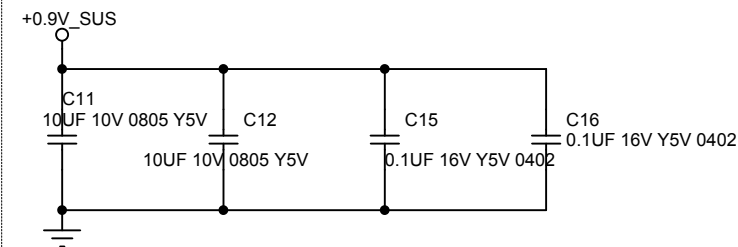
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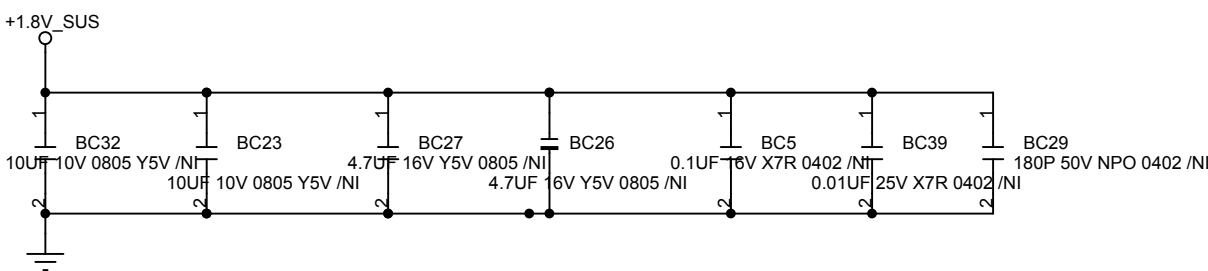
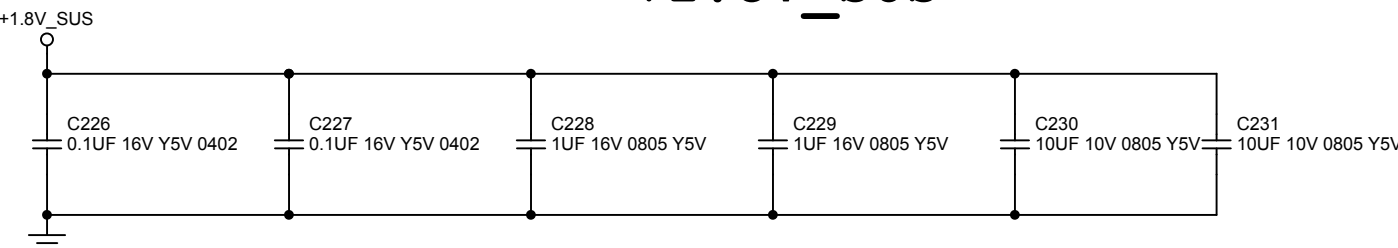
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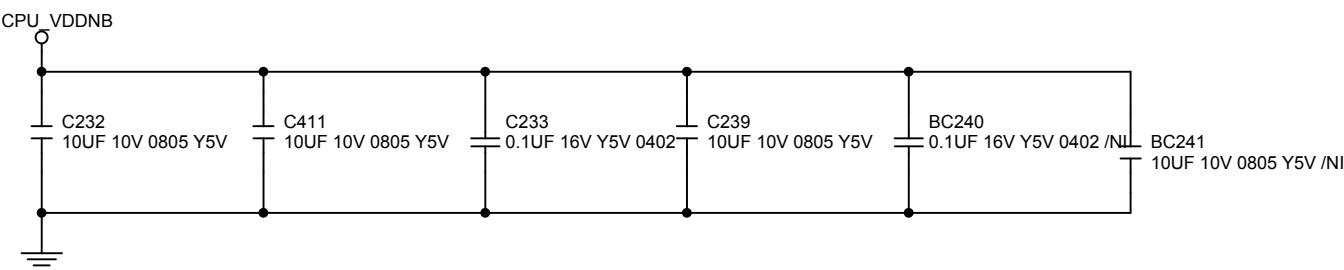
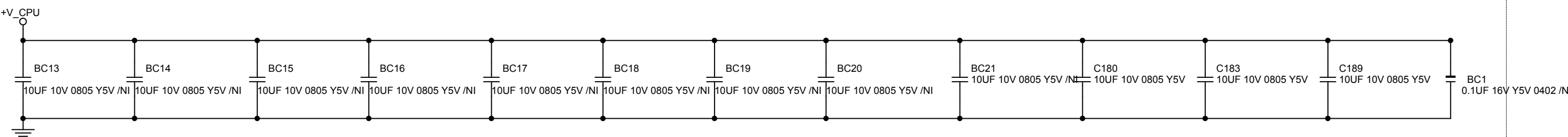
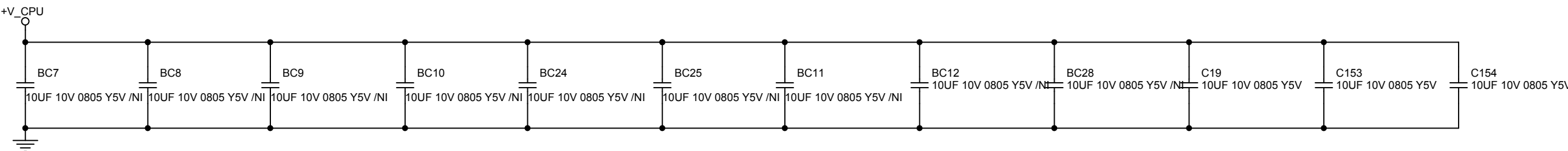
+0.9V\_SUS




+1.8V\_SUS



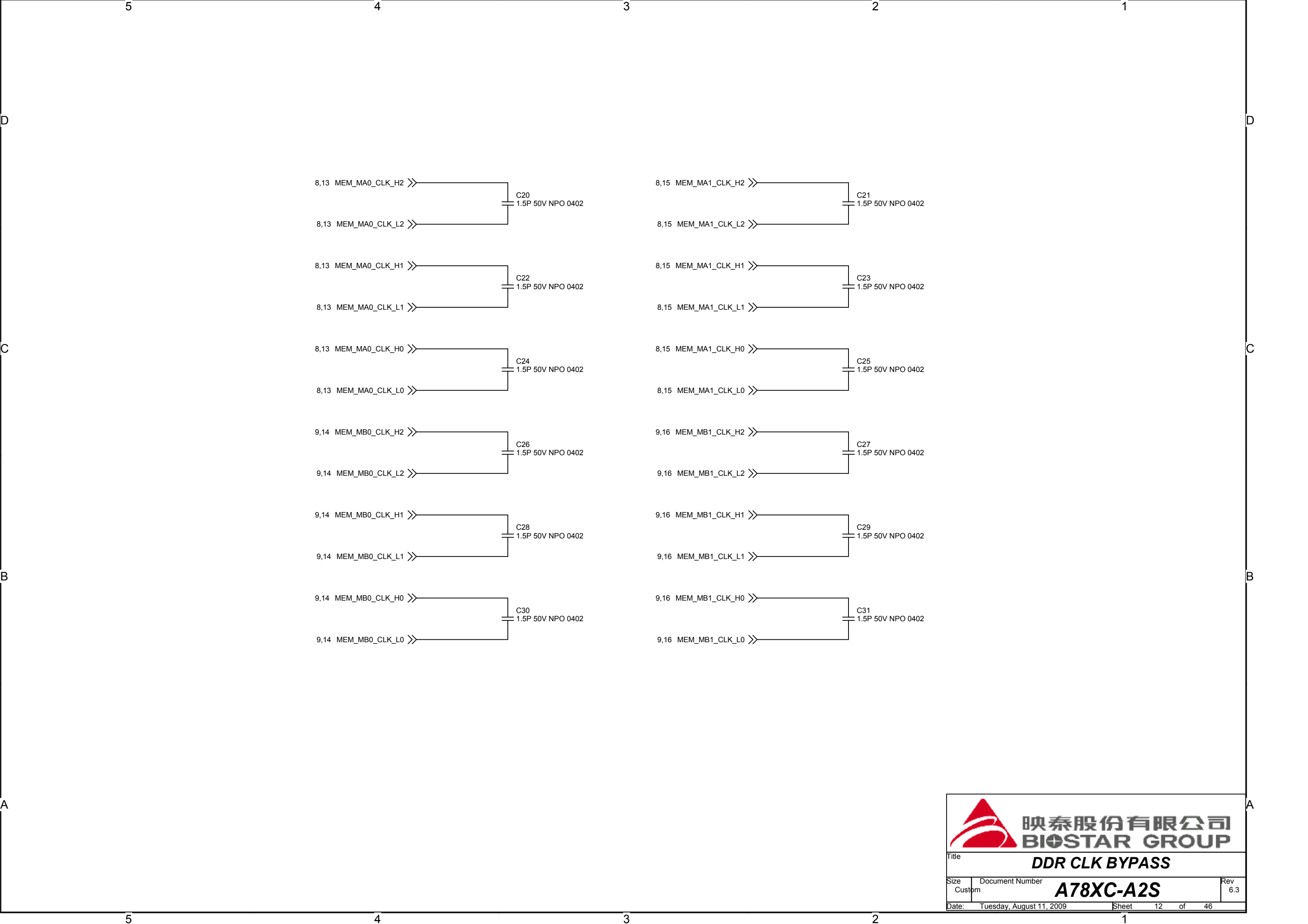
+V\_CPU

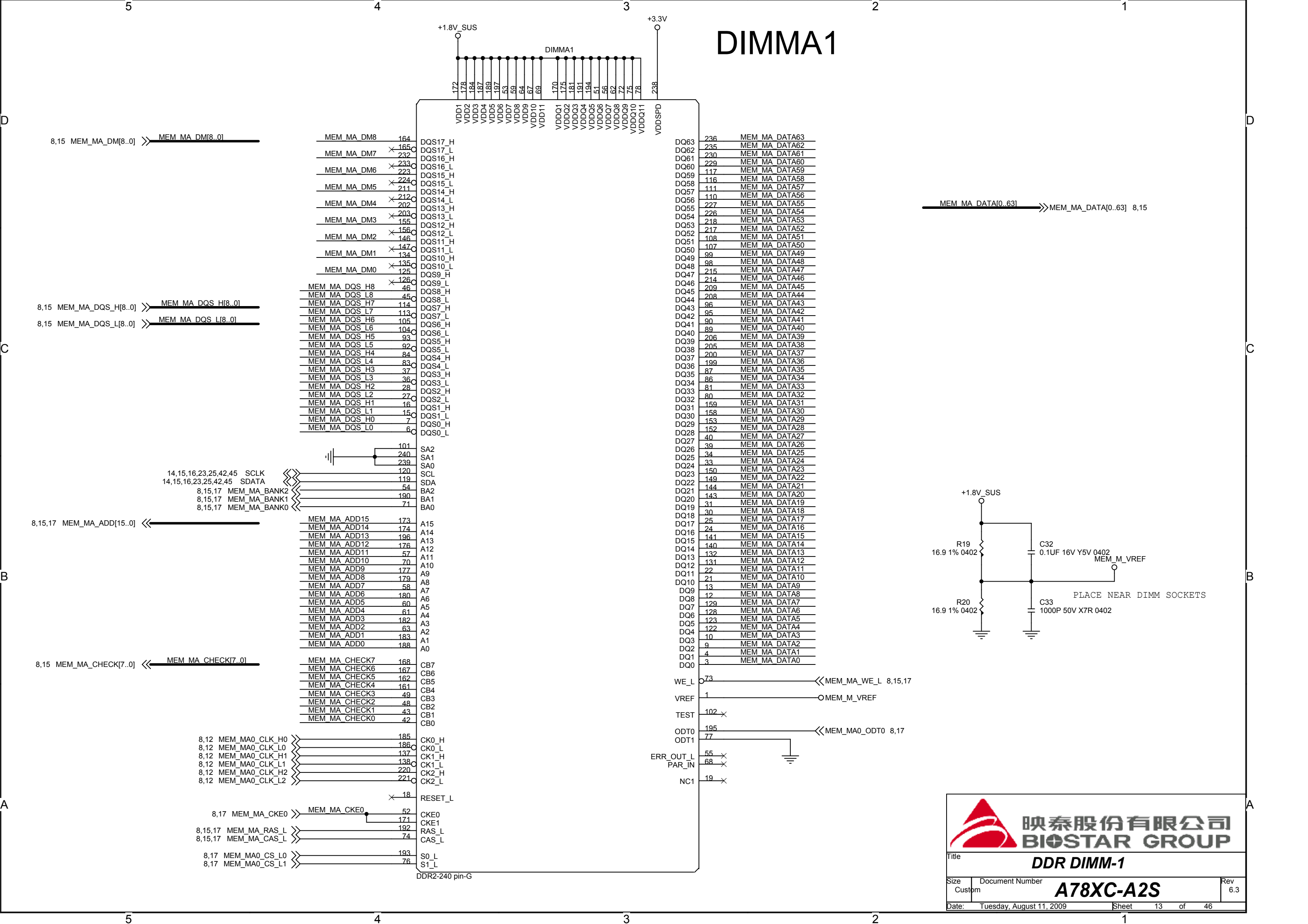




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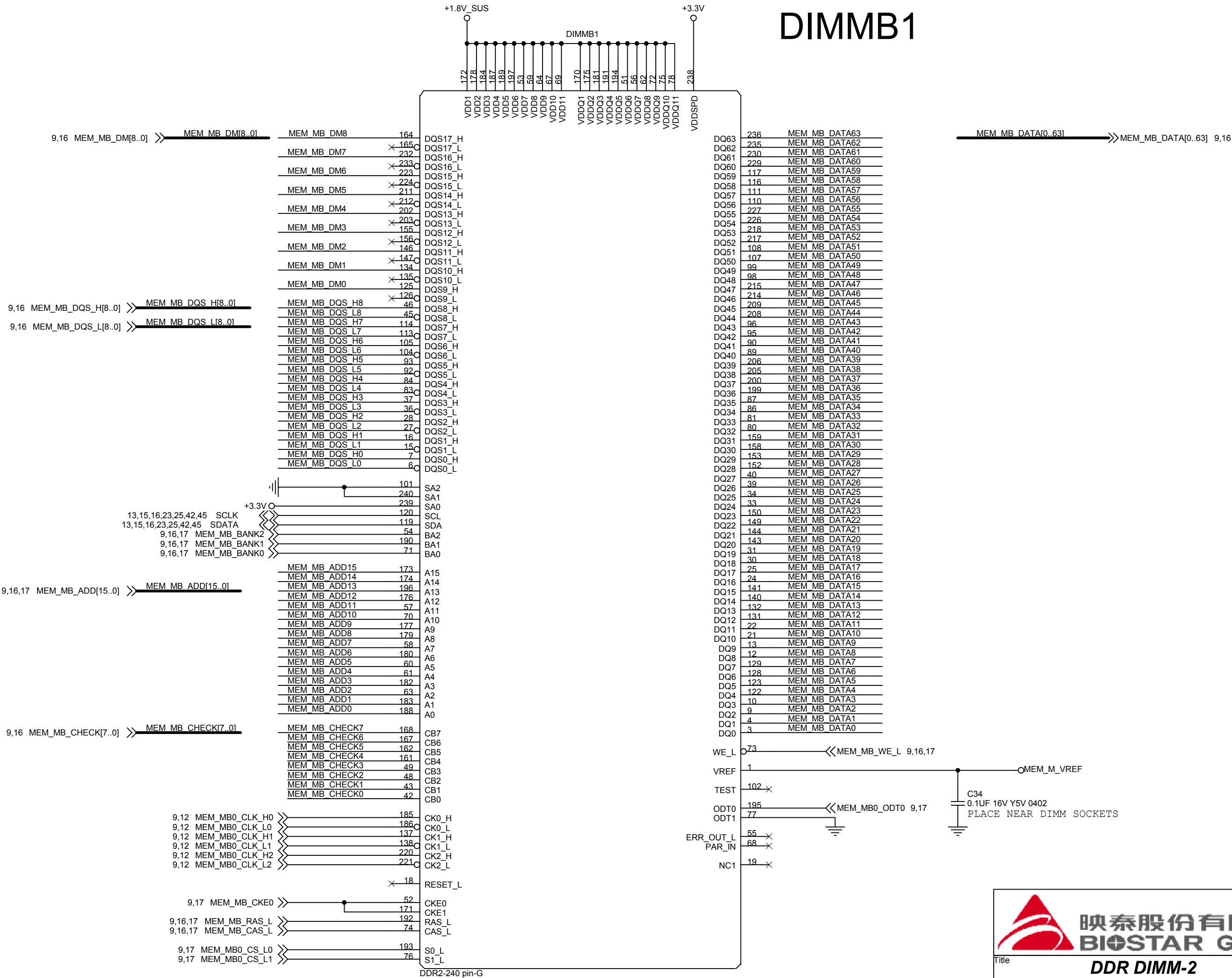
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Size	Document Number				Rev
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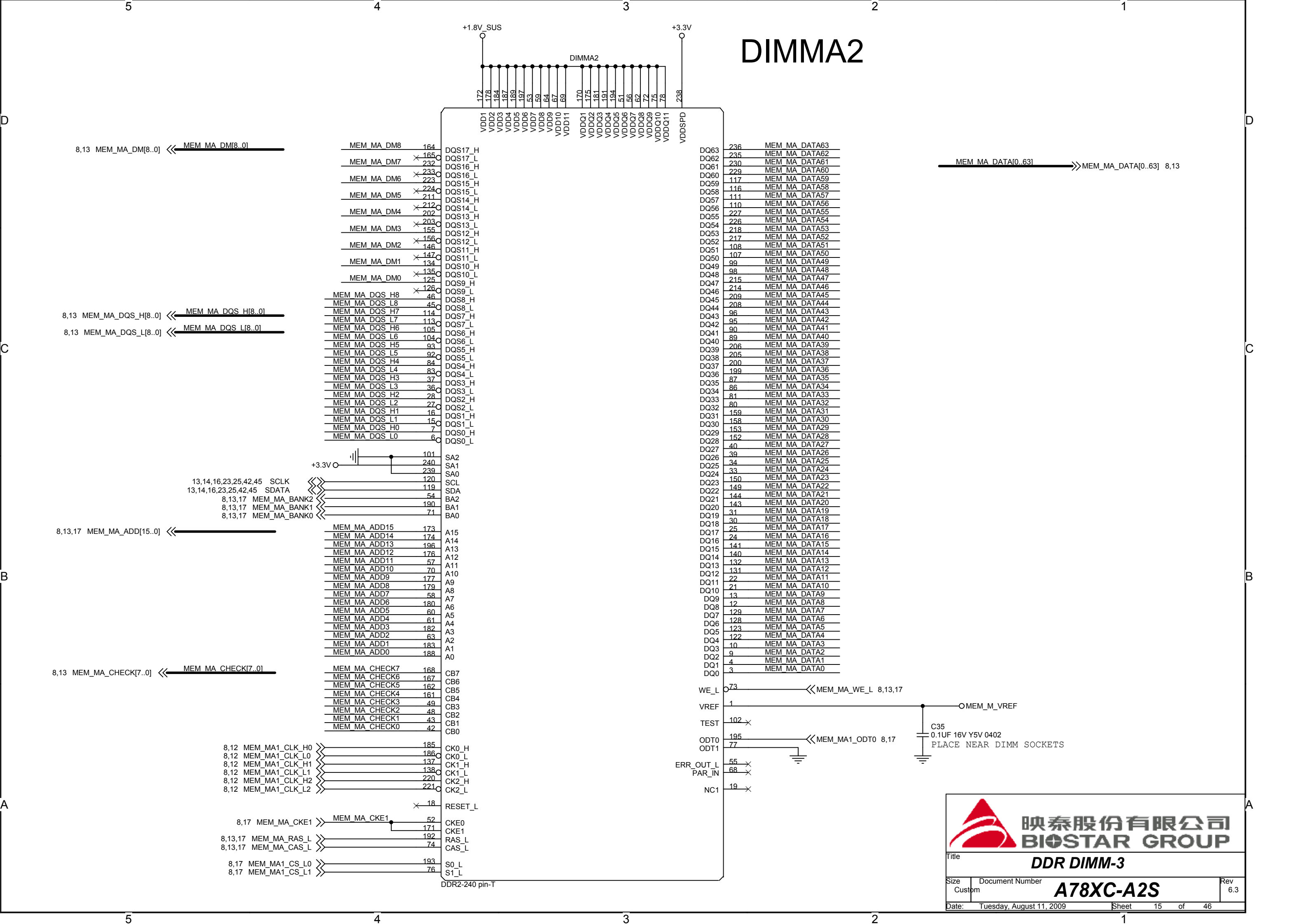




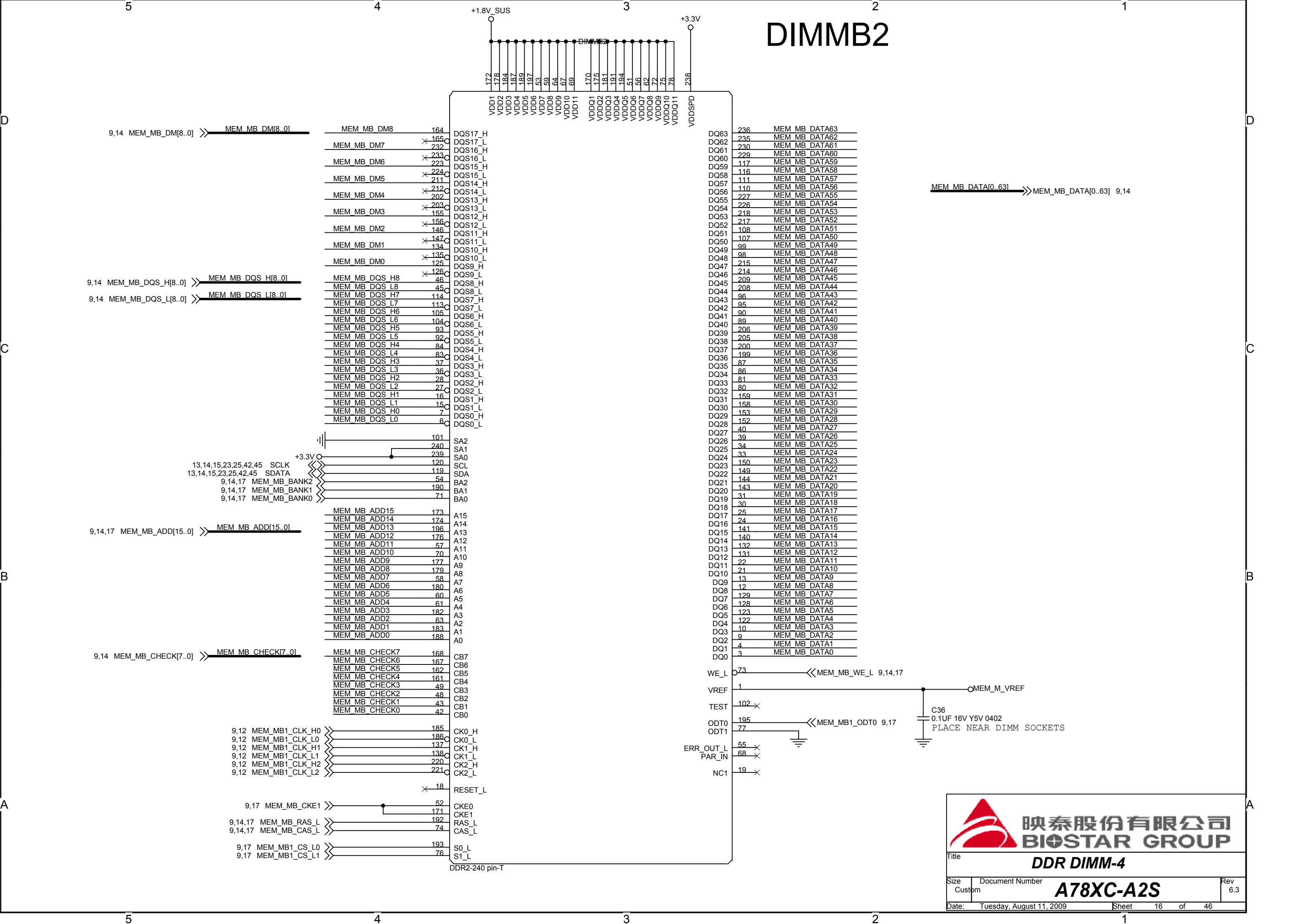
DIMMB1

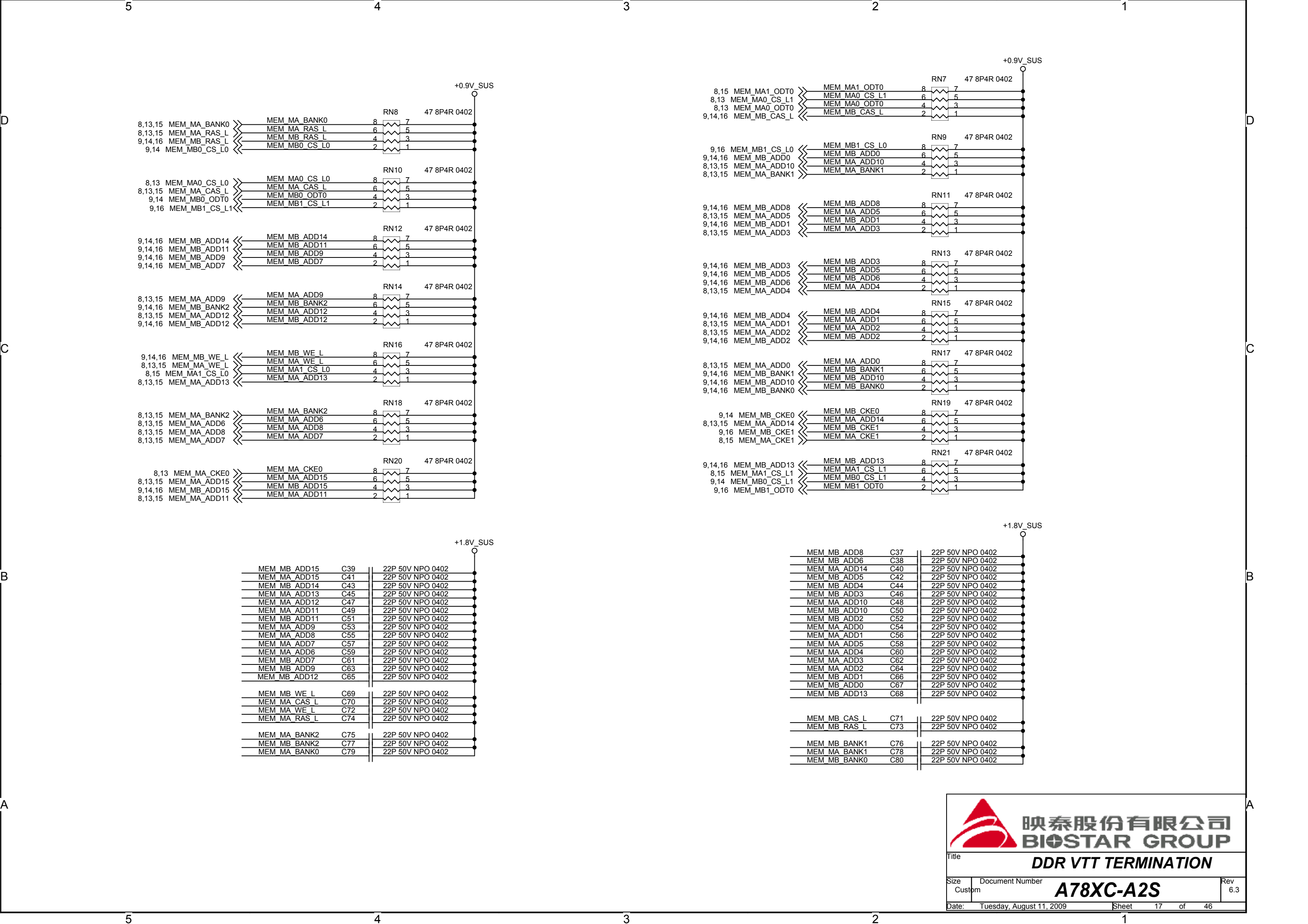


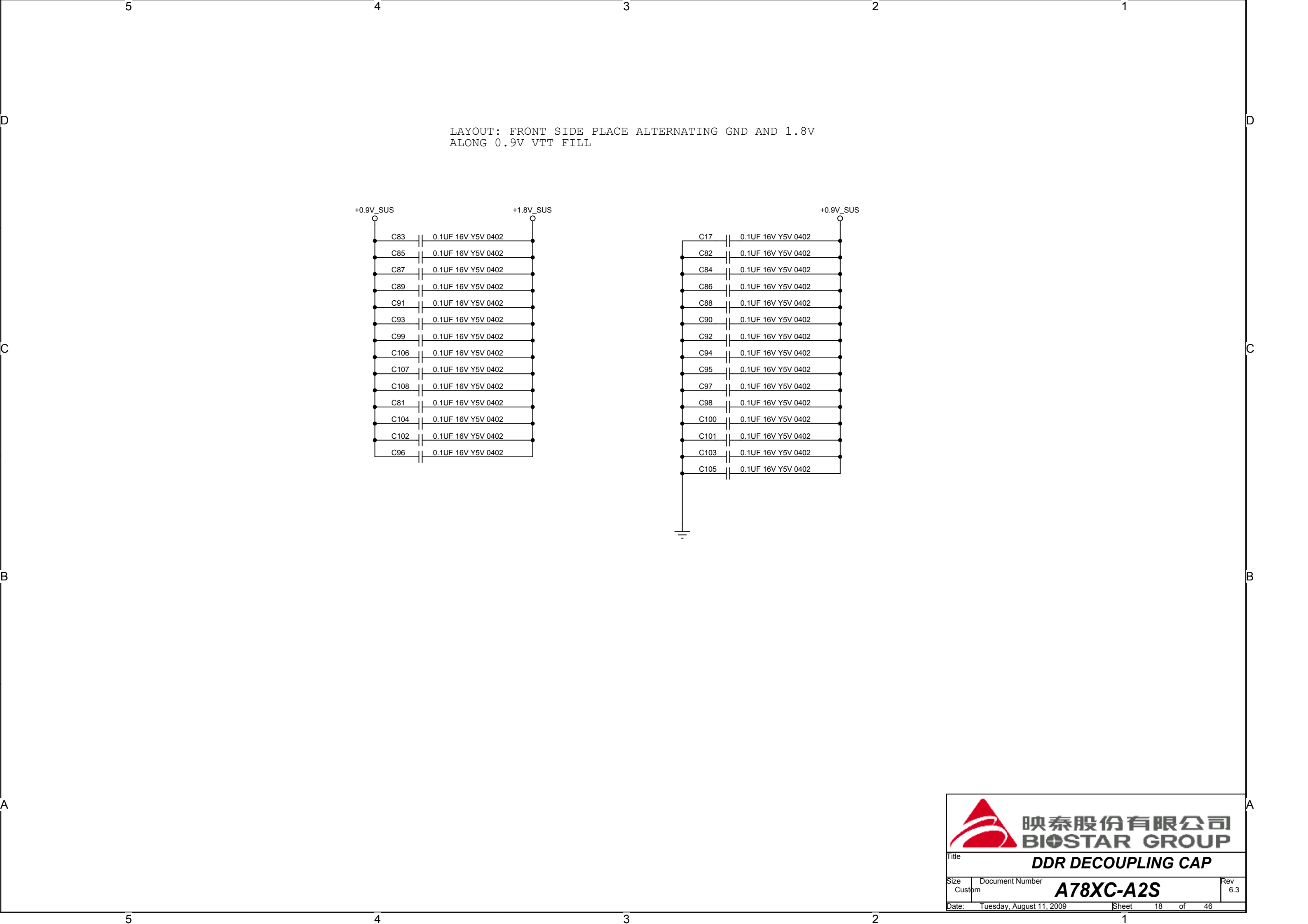
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Size	Document Number	A78XC-A2S	
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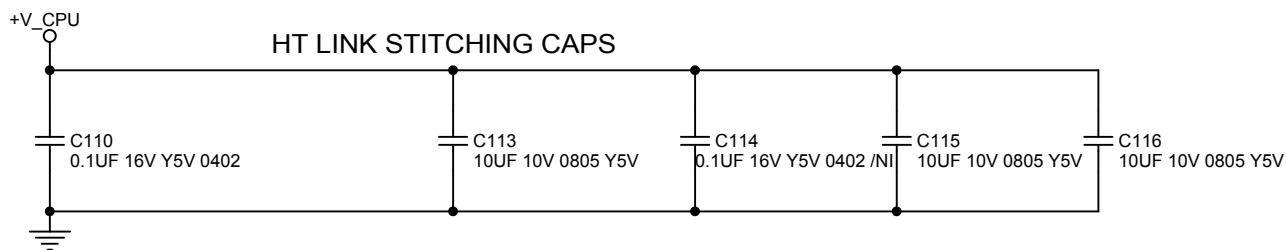
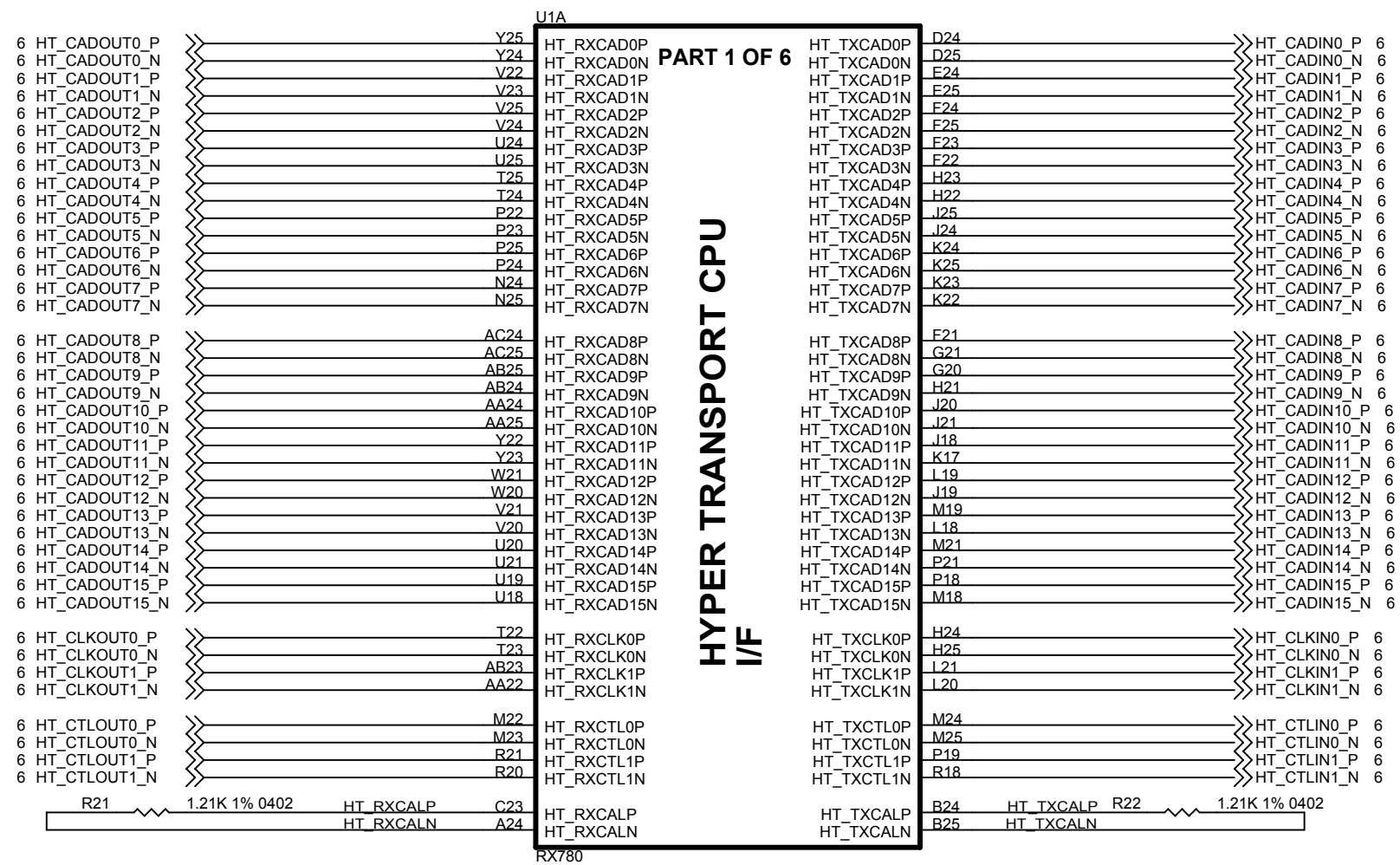








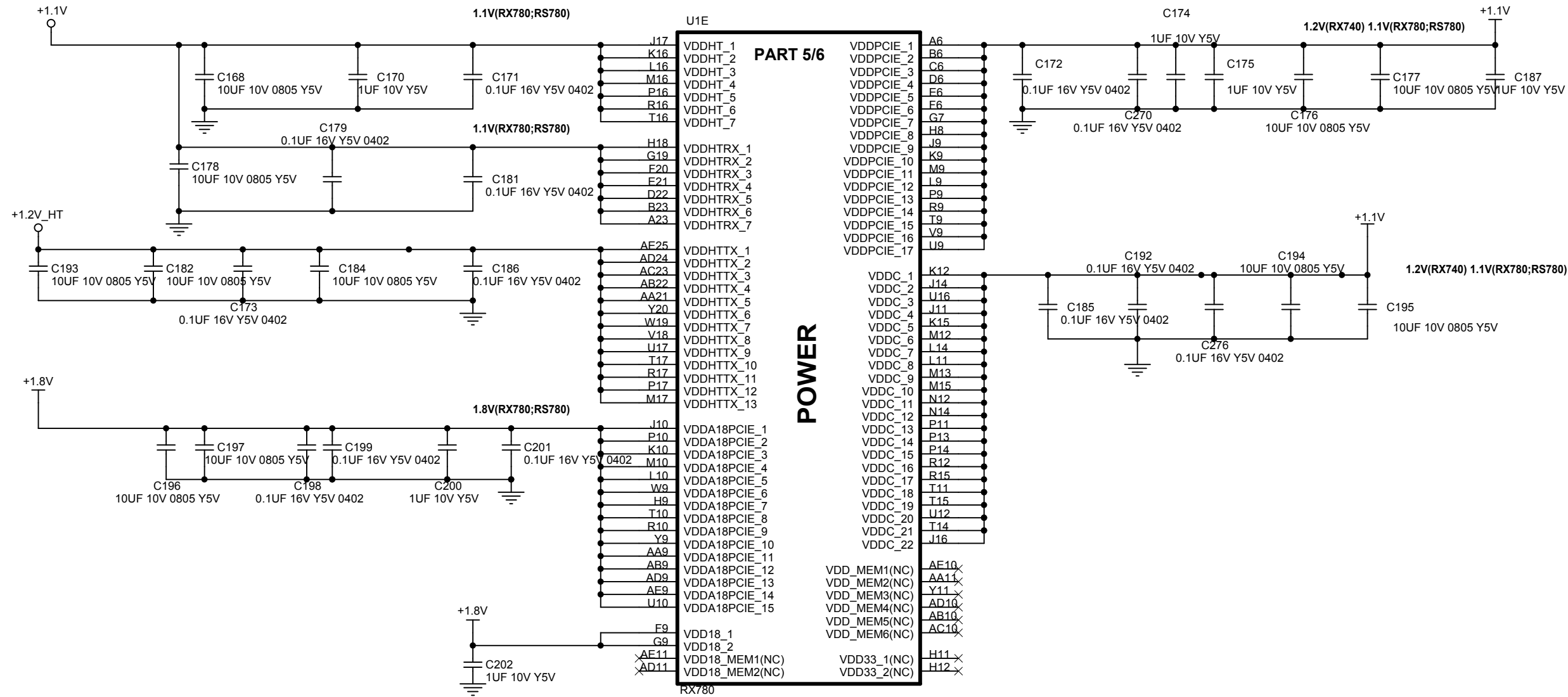
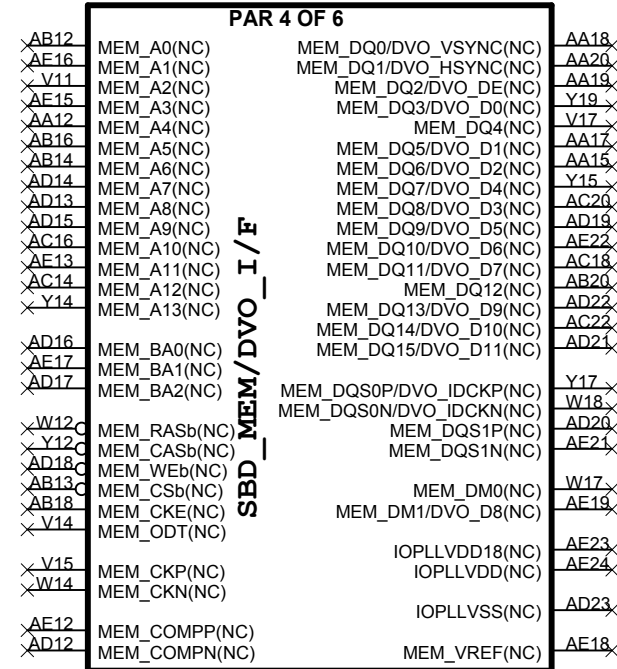
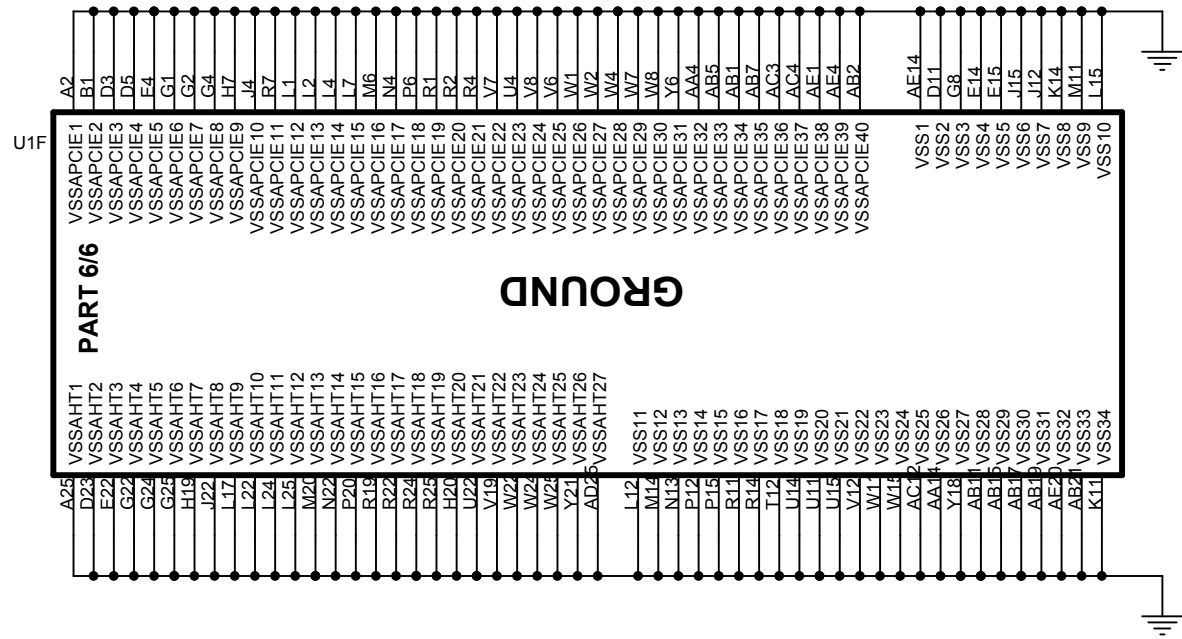






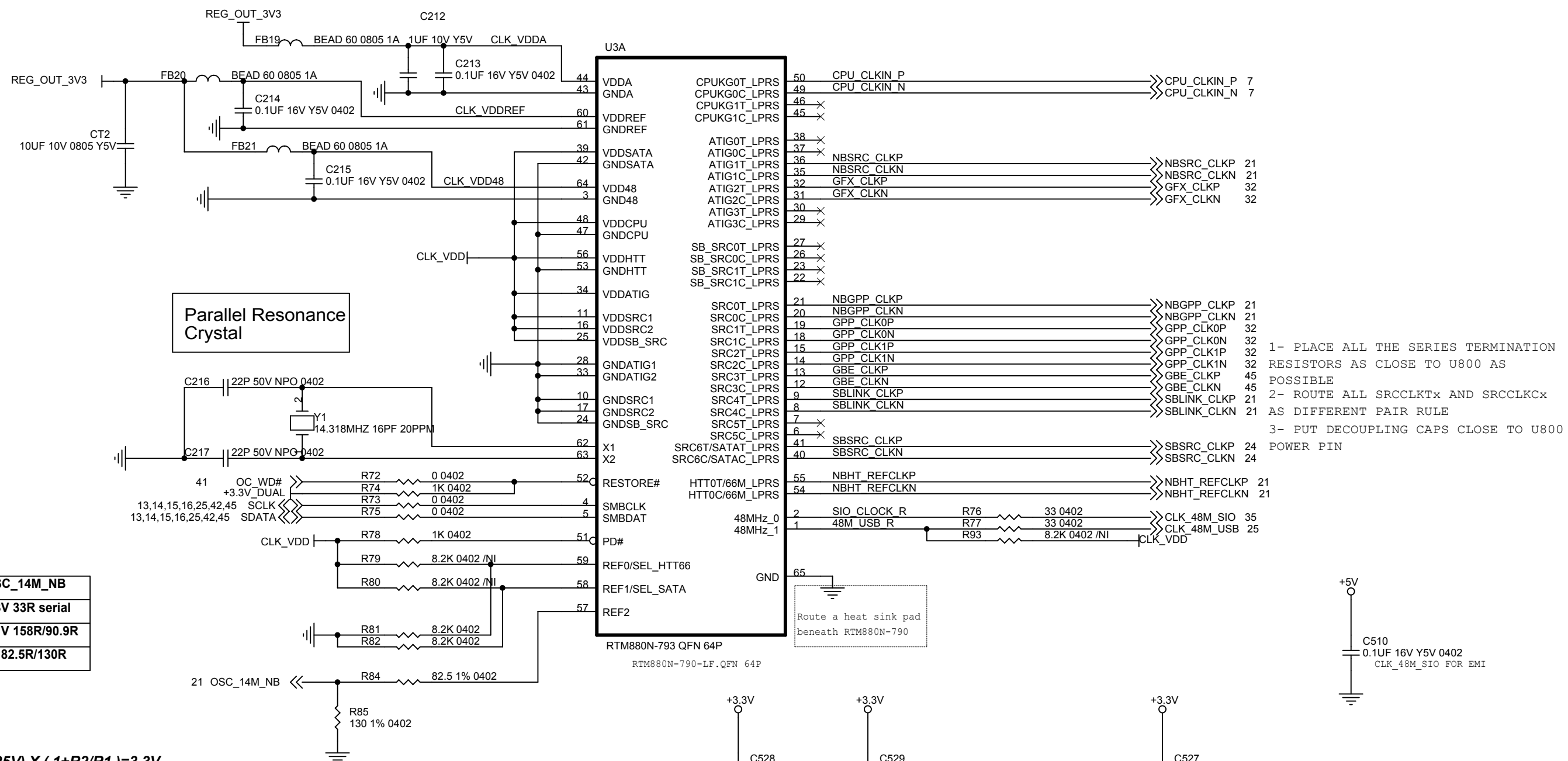






VDD18\_MEM only needed for RS780



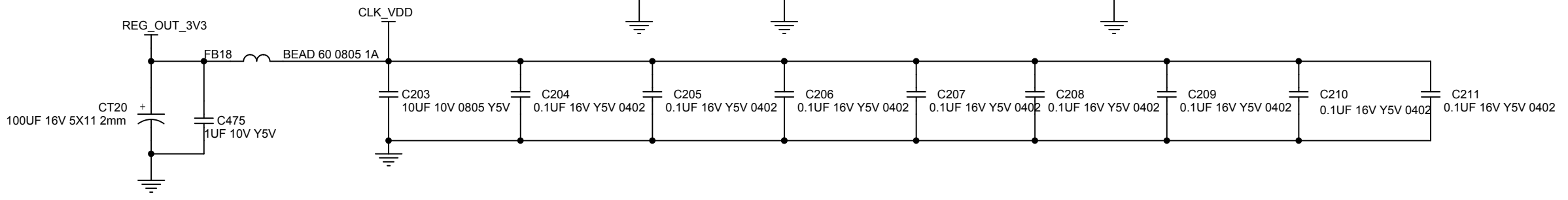
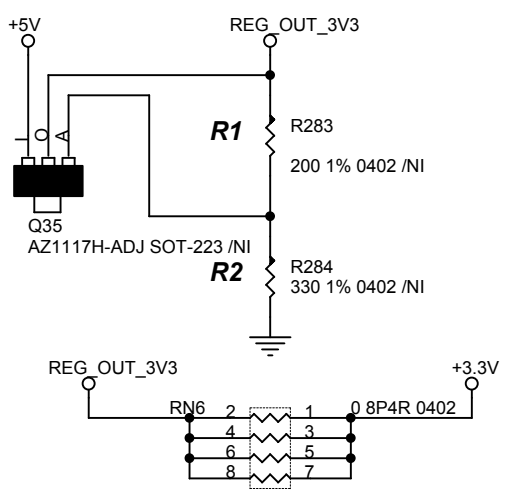


Parallel Resonance  
Crystal

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN


	OSC_14M_NB
RS740	3.3V 33R serial
RS780	1.1V 158R/90.9R
RX780	1.8V 82.5R/130R

$V_{out} = V_{ref} (1.25V) \times (1 + R2/R1) = 3.3V$



SEL_HTT66	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock
SEL_SATA	1*	100MHz non-spreading differential SATA clock
	0	100MHz differential spreading SRC clock

\* default



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Title  
**CLOCK GEN**

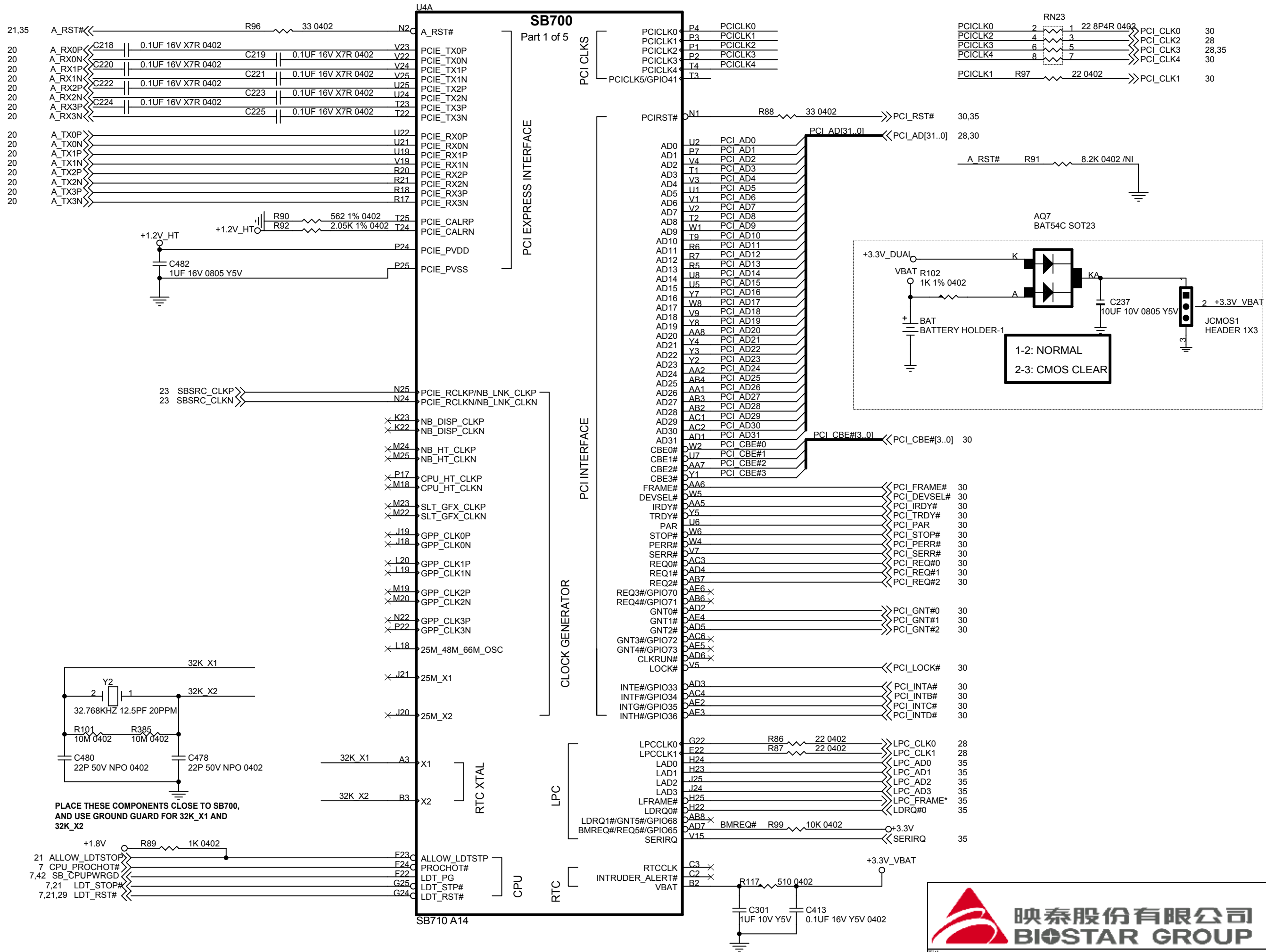
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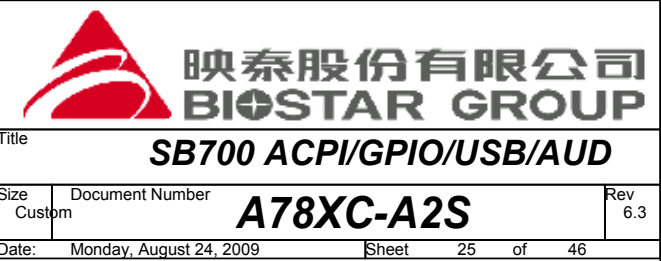
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**A78XC-A2S**

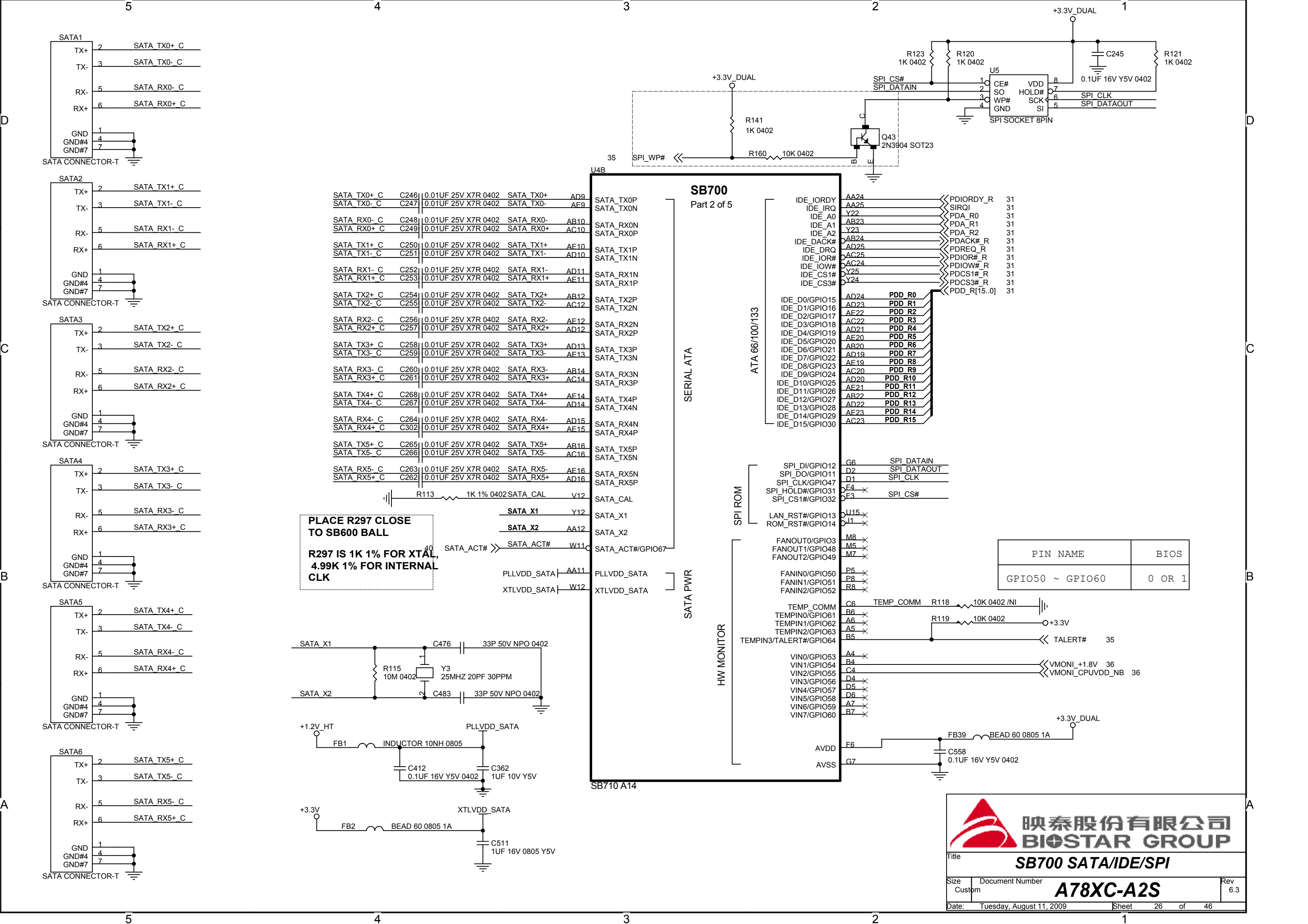
Date: Tuesday, August 11, 2009

Rev  
6.3

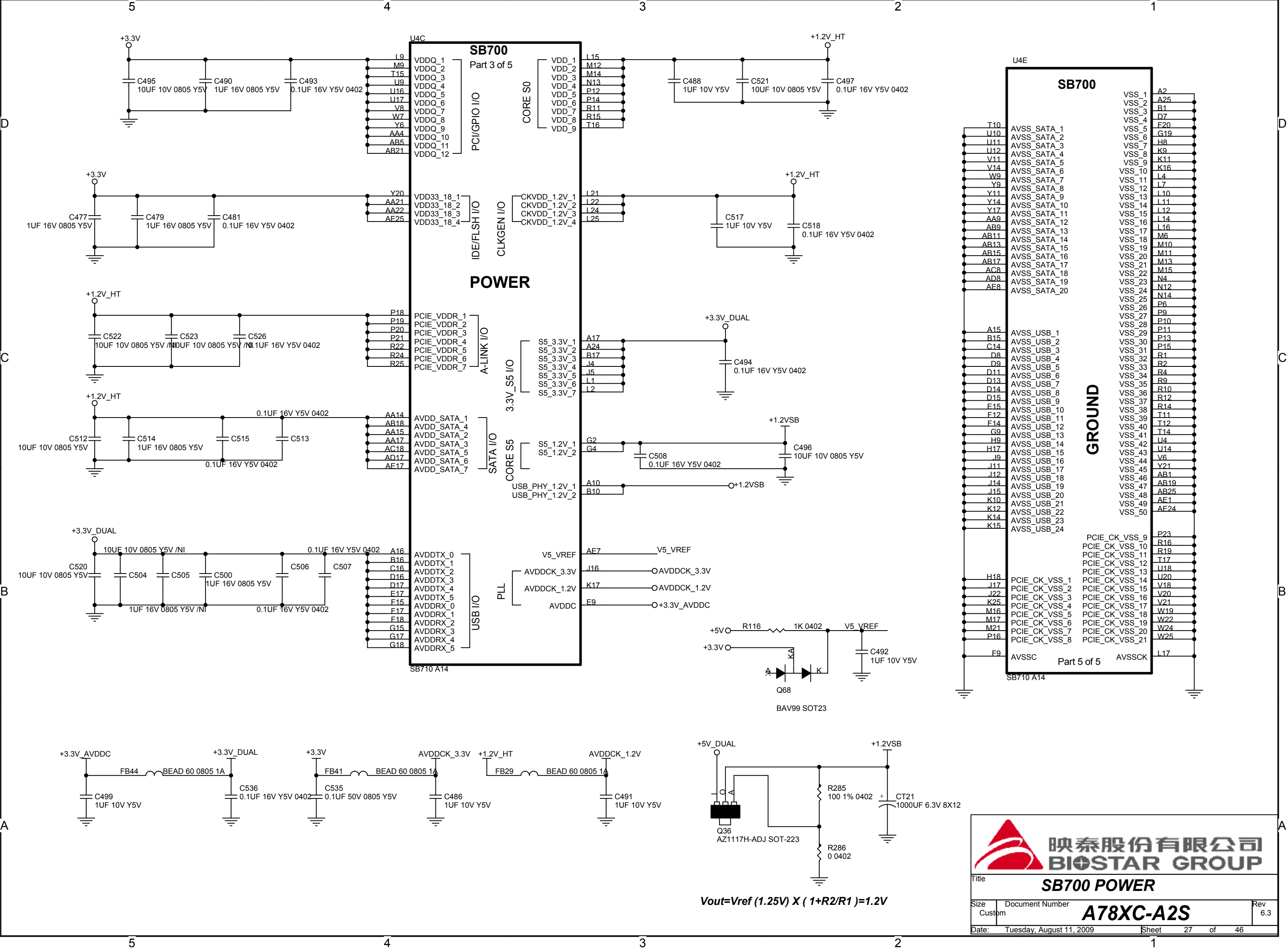
Sheet 23 of 46



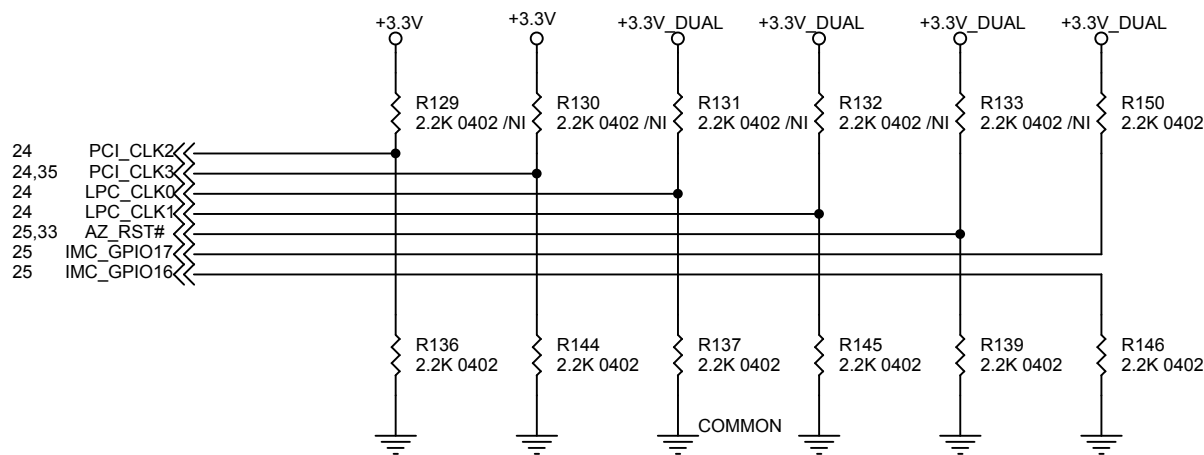








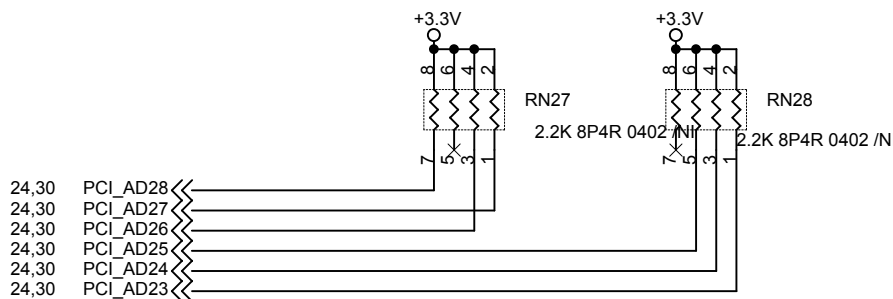
REQUIRED STRAPS



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC\_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17 IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, L = SPI ROM
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	DEFAULT

DEBUG STRAPS



SB700 HAS 15K INTERNAL PU FOR PCI\_AD[28:23]

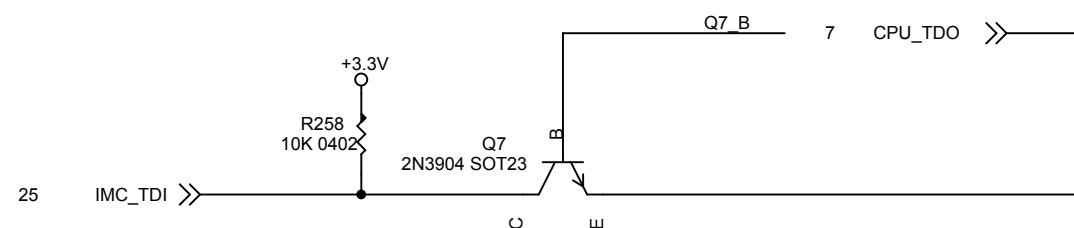
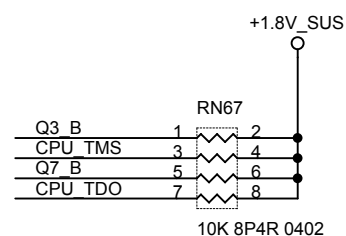
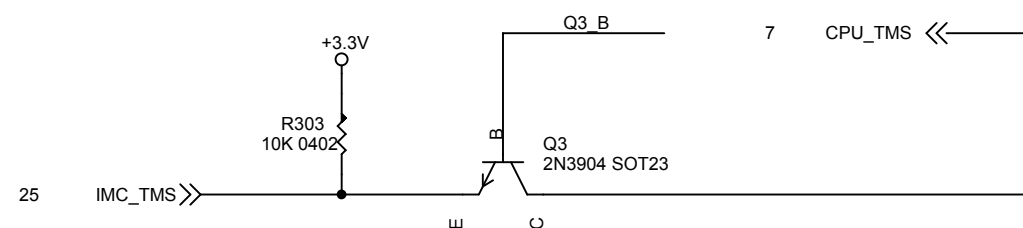
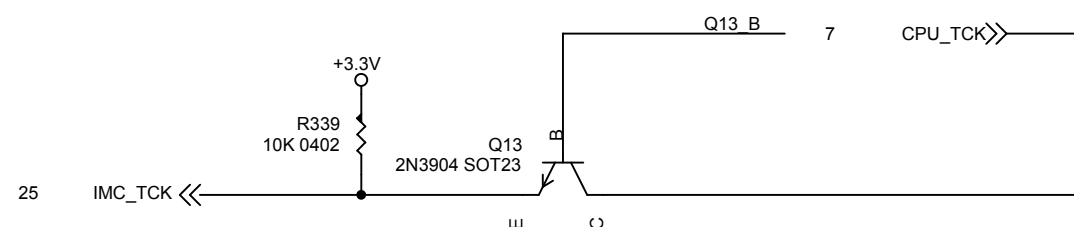
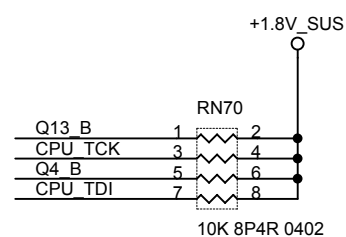
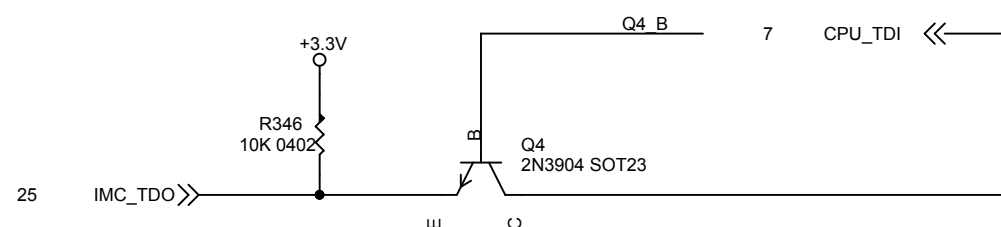
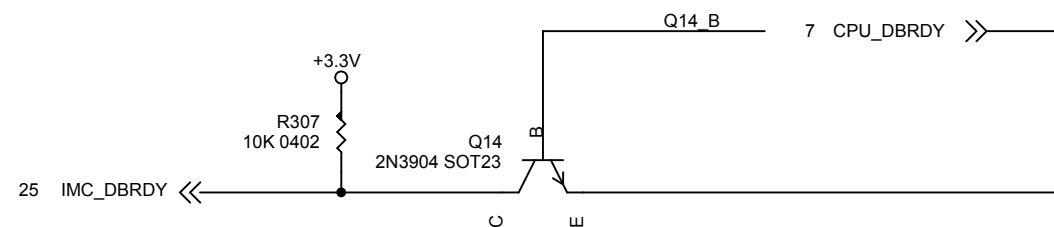
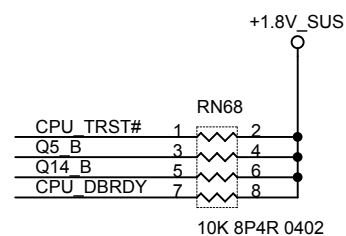
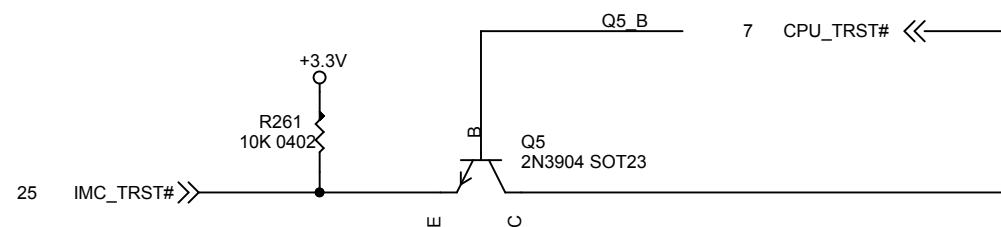
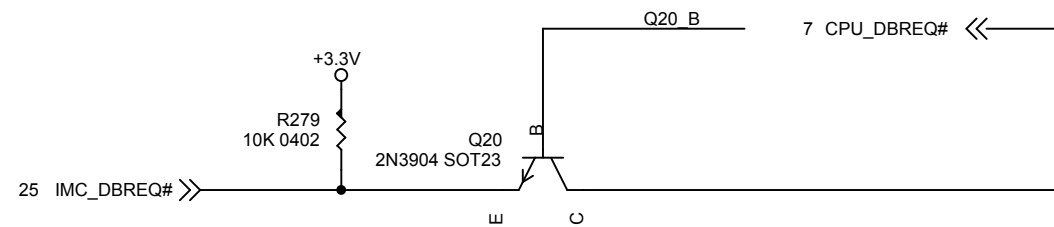
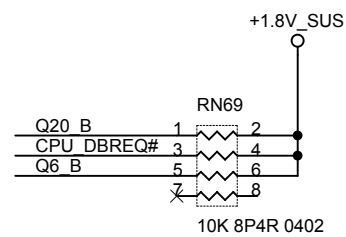
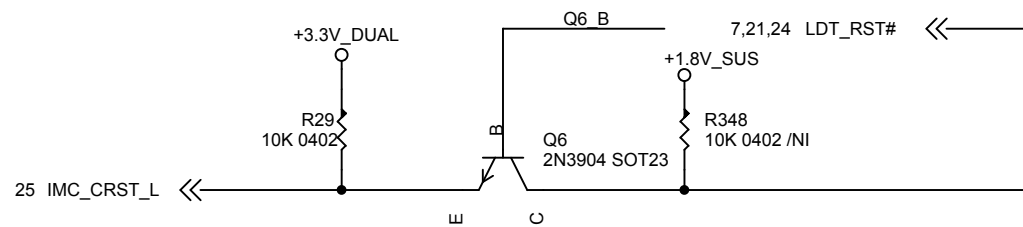
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

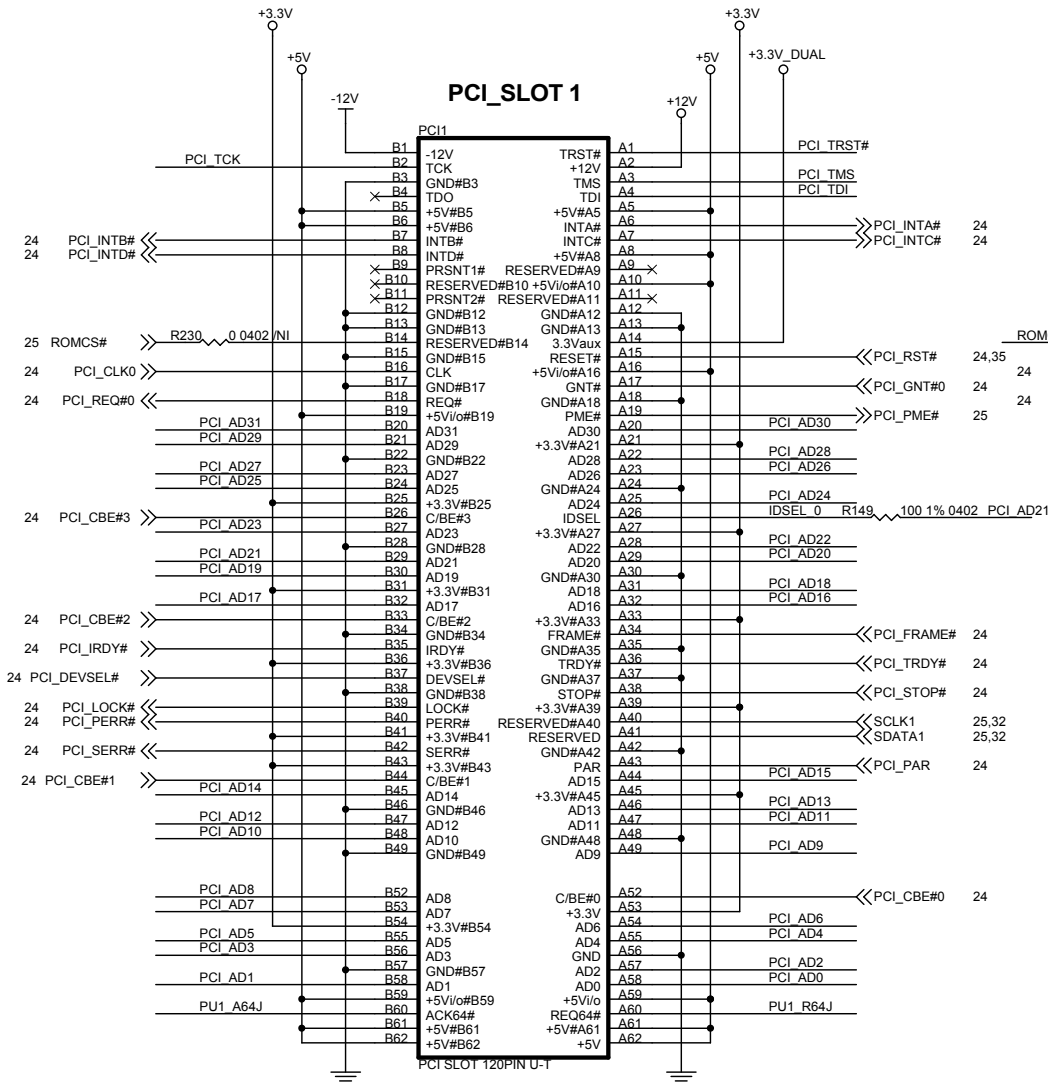


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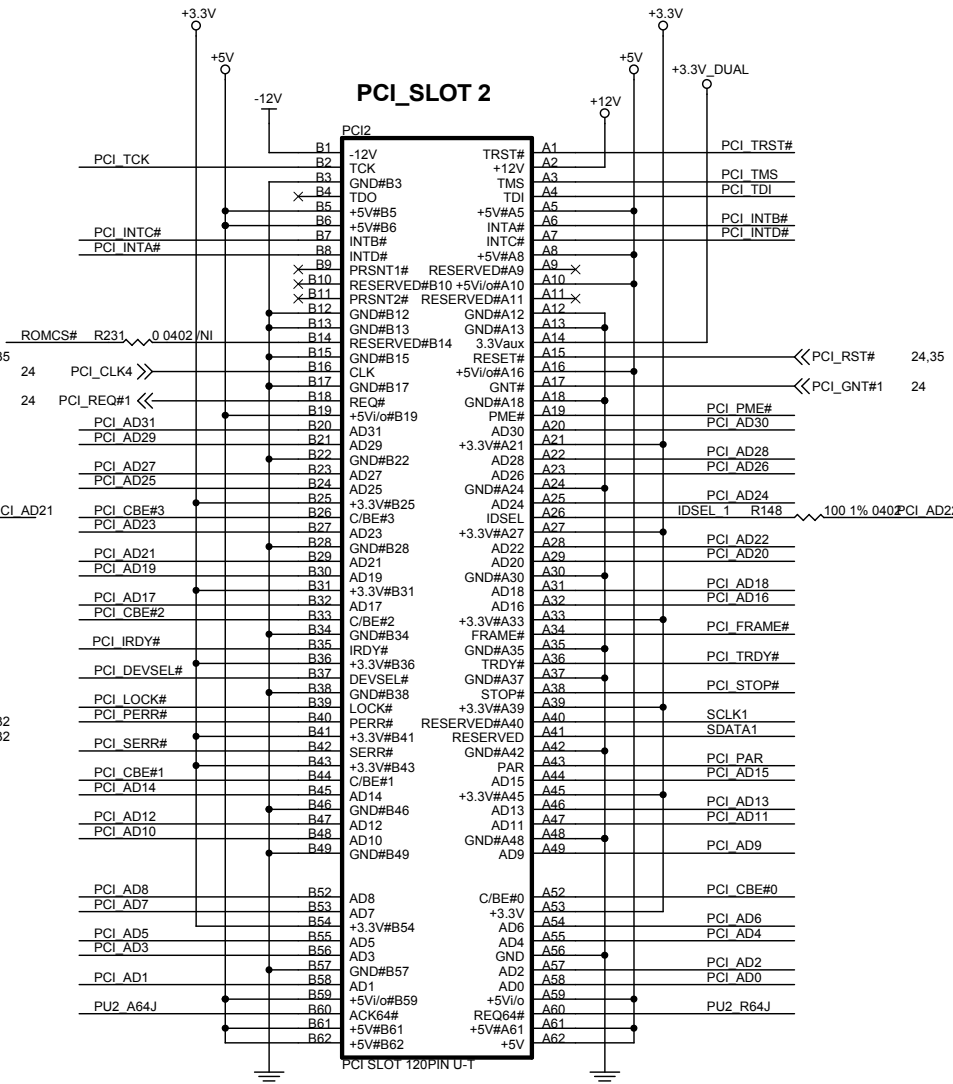




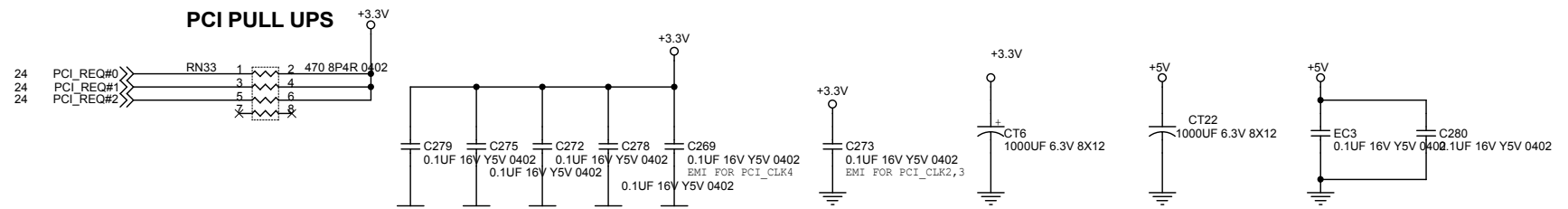
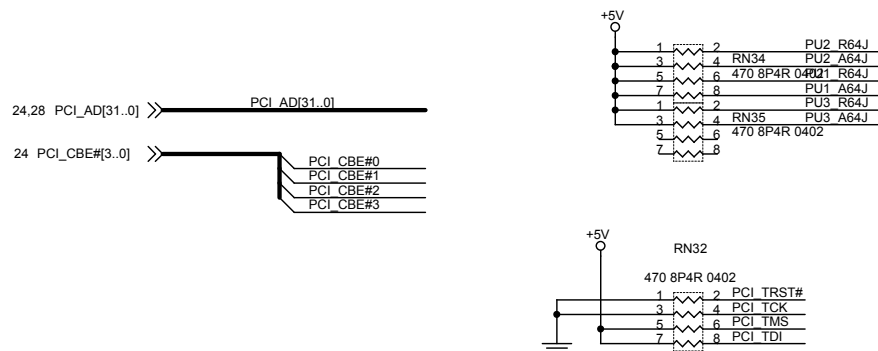
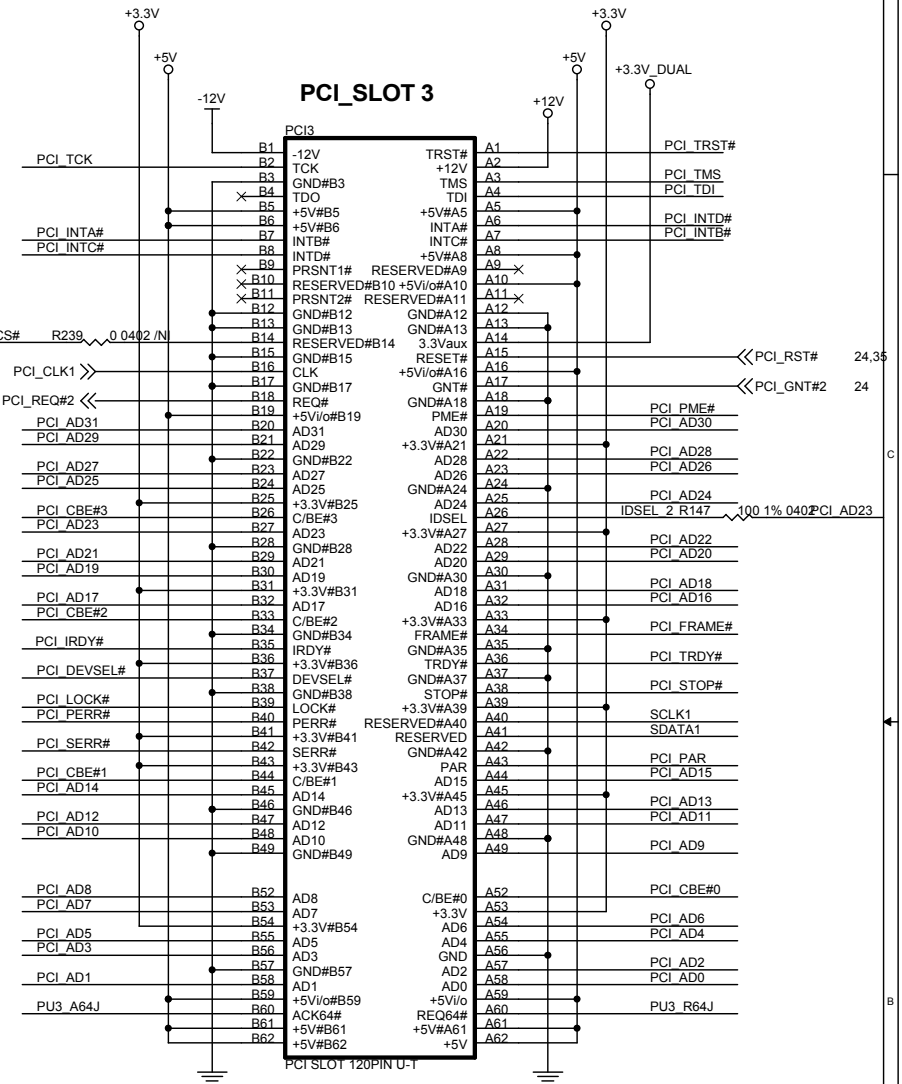
IDSEL:AD21, INT:ABCD, REQ0 &amp; GNT0, PCI\_CLK3



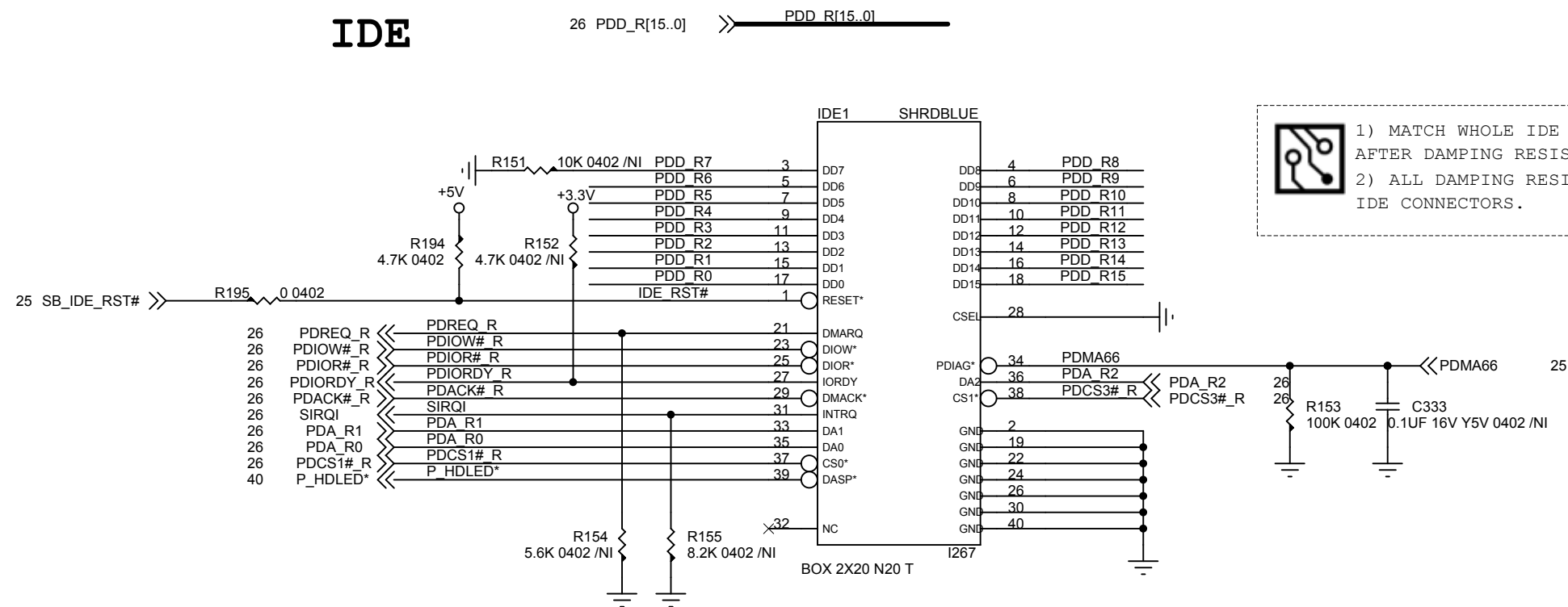
IDSEL:AD22, INT:BCDA, REQ1 &amp; GNT1, PCI\_CLK4



IDSEL:AD23, INT:DABC, REQ2 &amp; GNT2, PCI\_CLK2

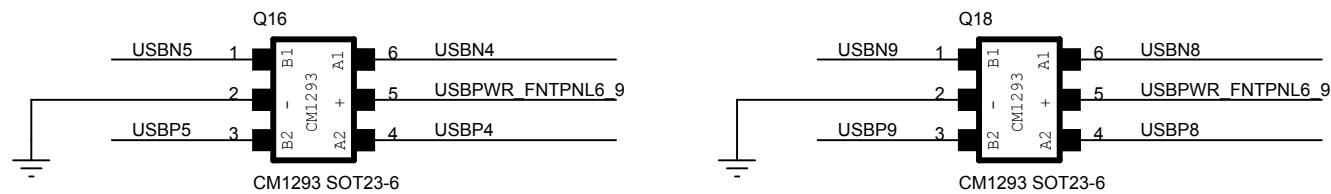
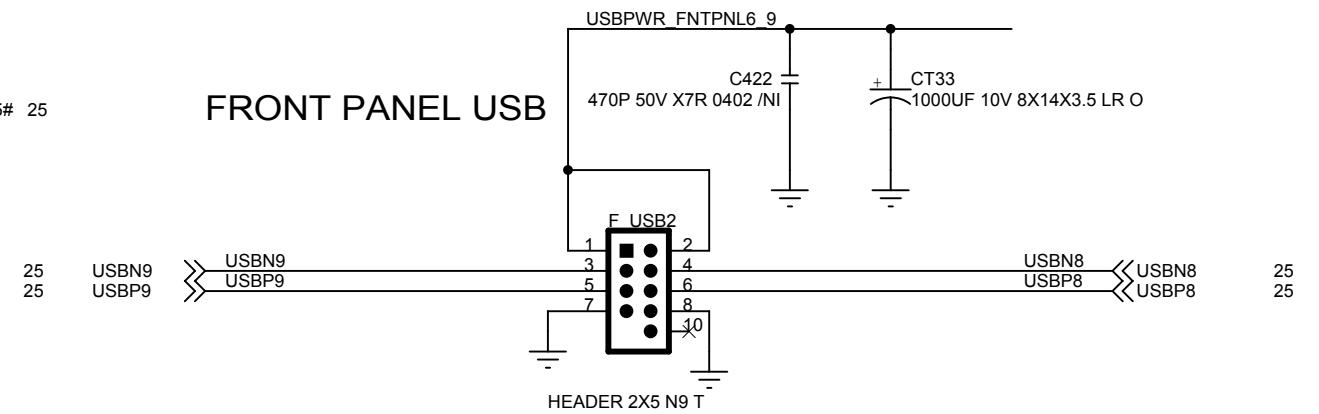
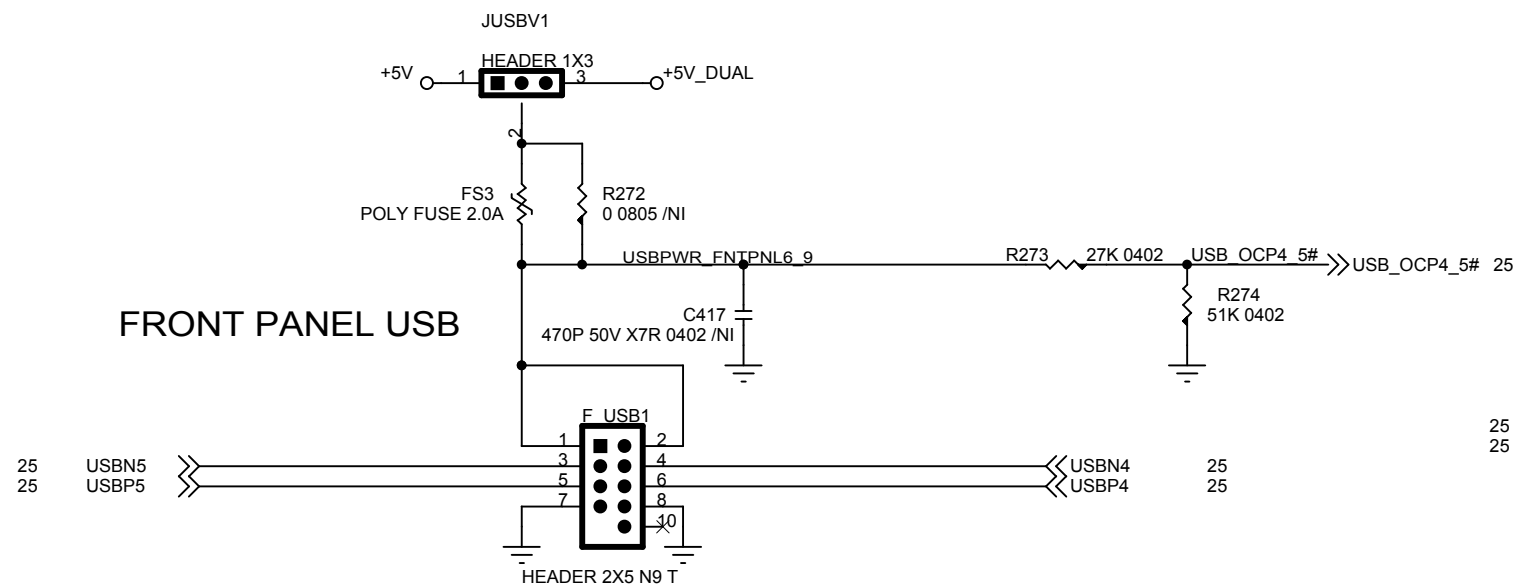


# IDE



- 1) MATCH WHOLE IDE LINES (BEFORE AND AFTER DAMPING RESISTORS) WITHIN 0.5"
- 2) ALL DAMPING RESISTORS CLOSE TO IDE CONNECTORS.

**FORNT USB**

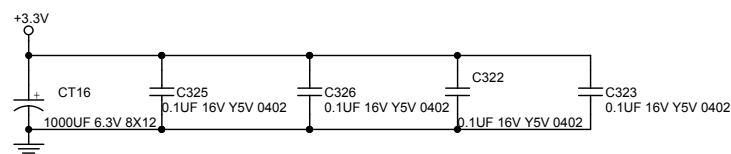
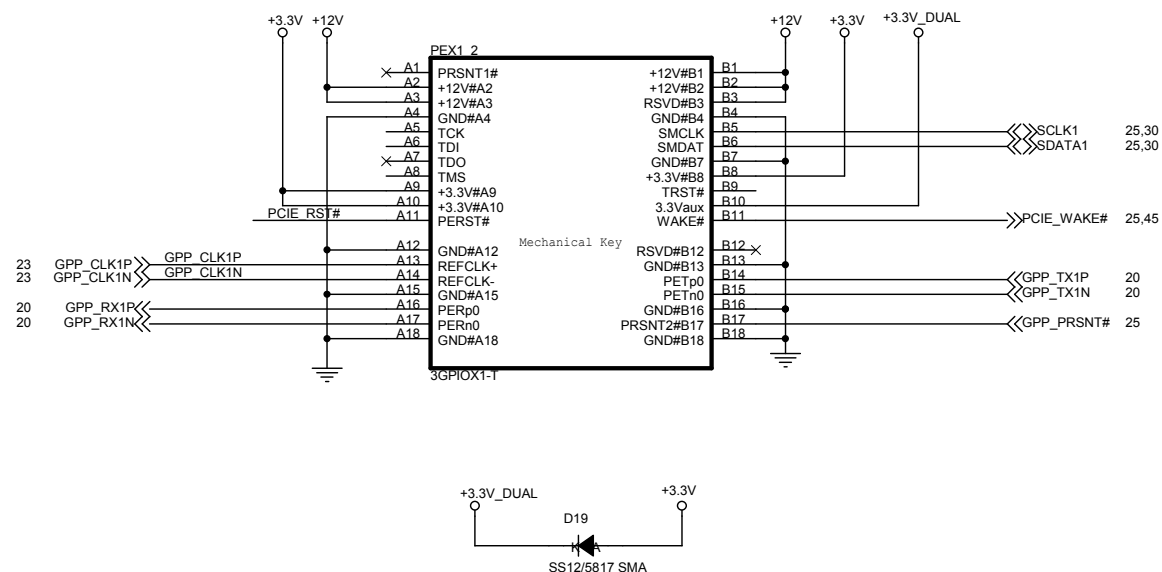
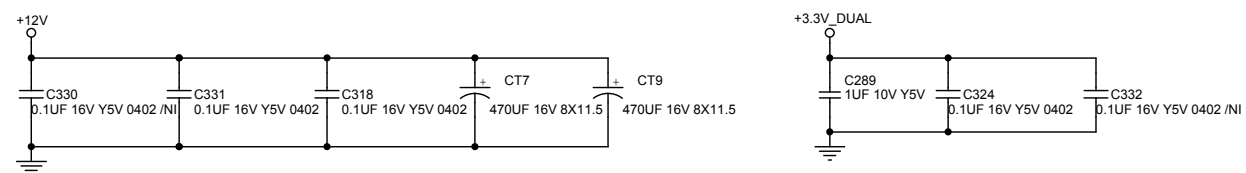
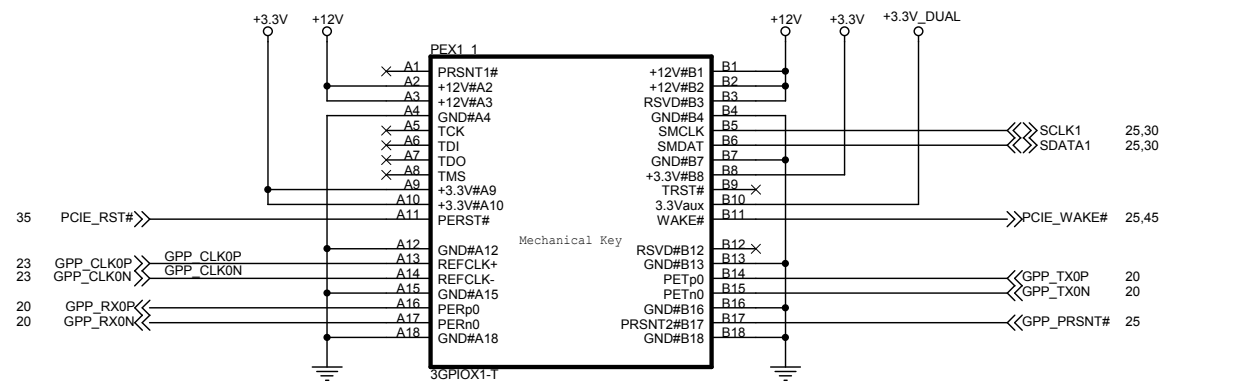
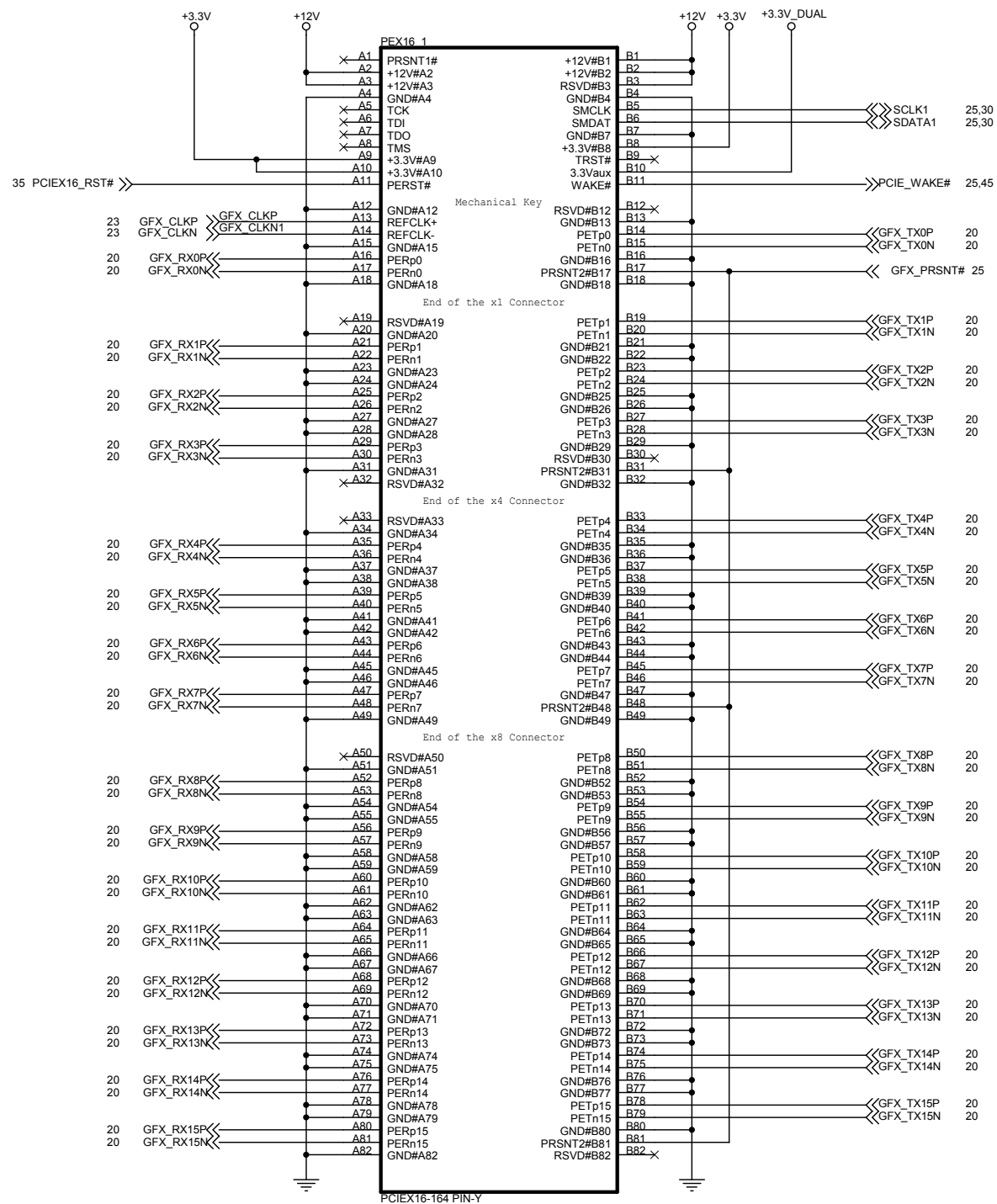


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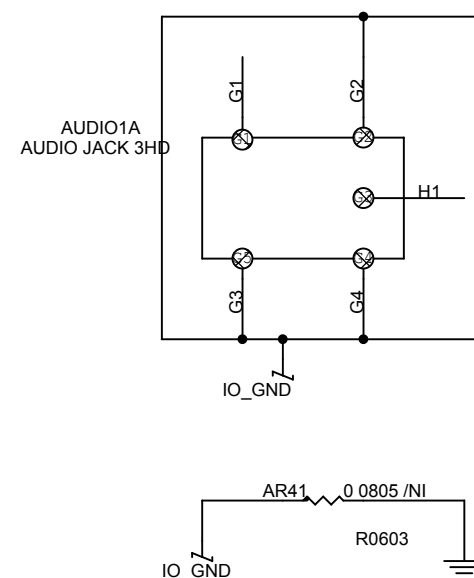
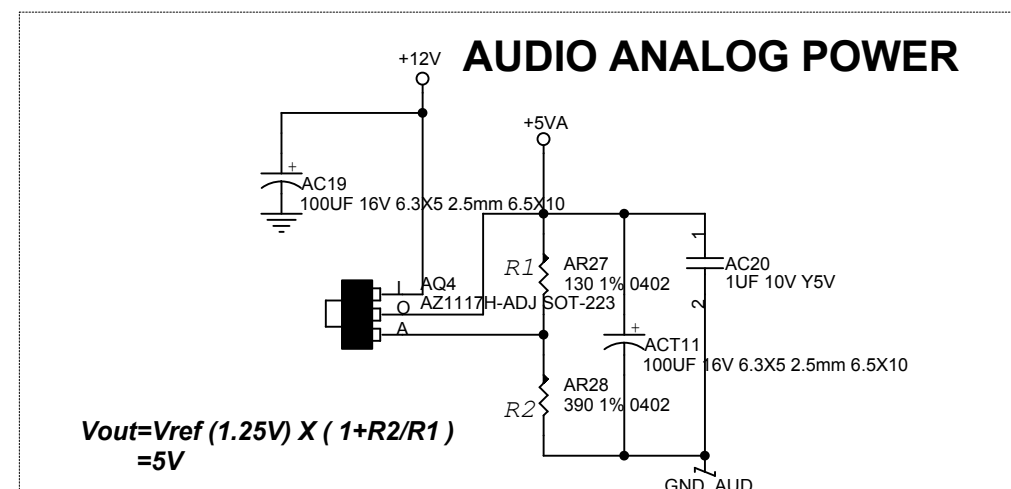
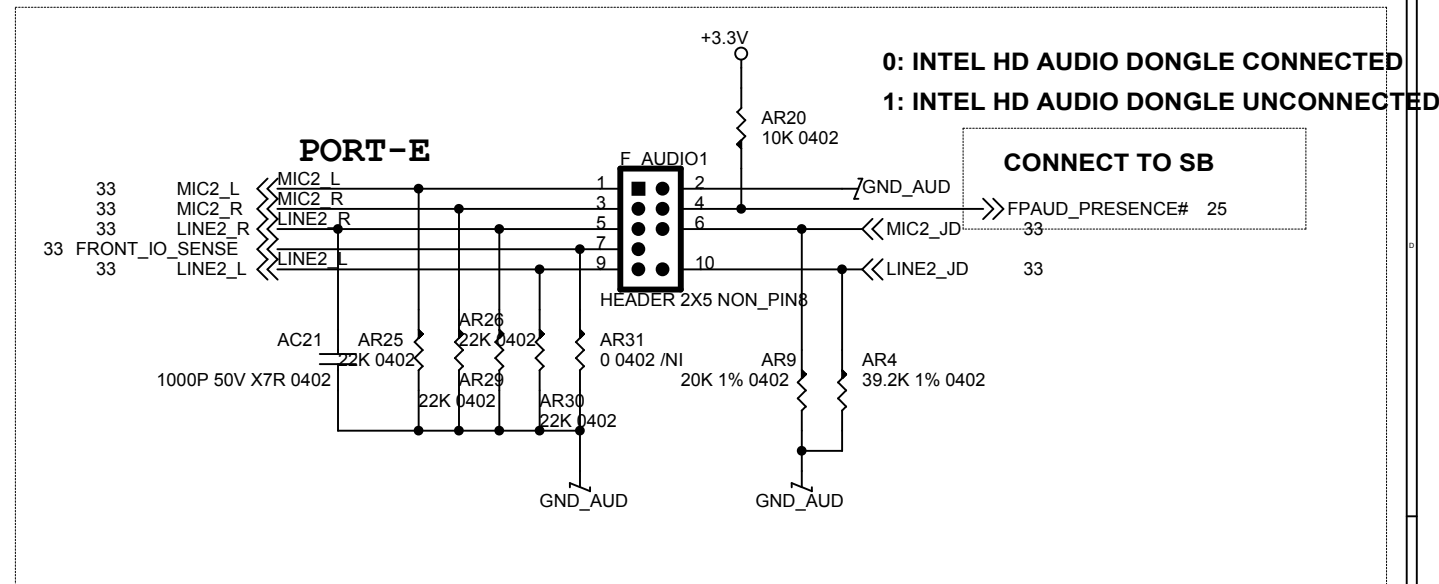
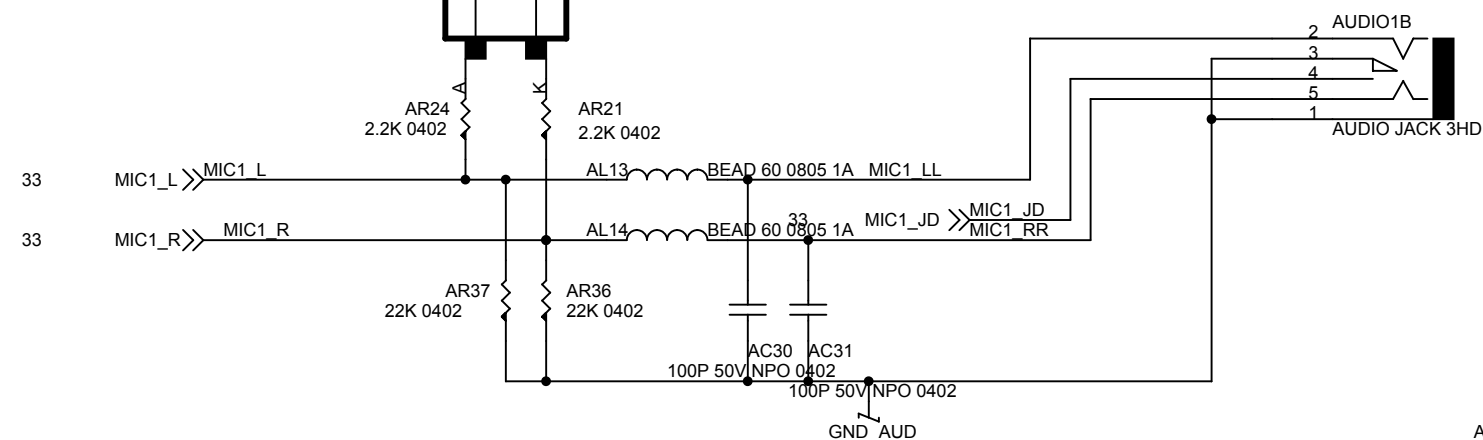
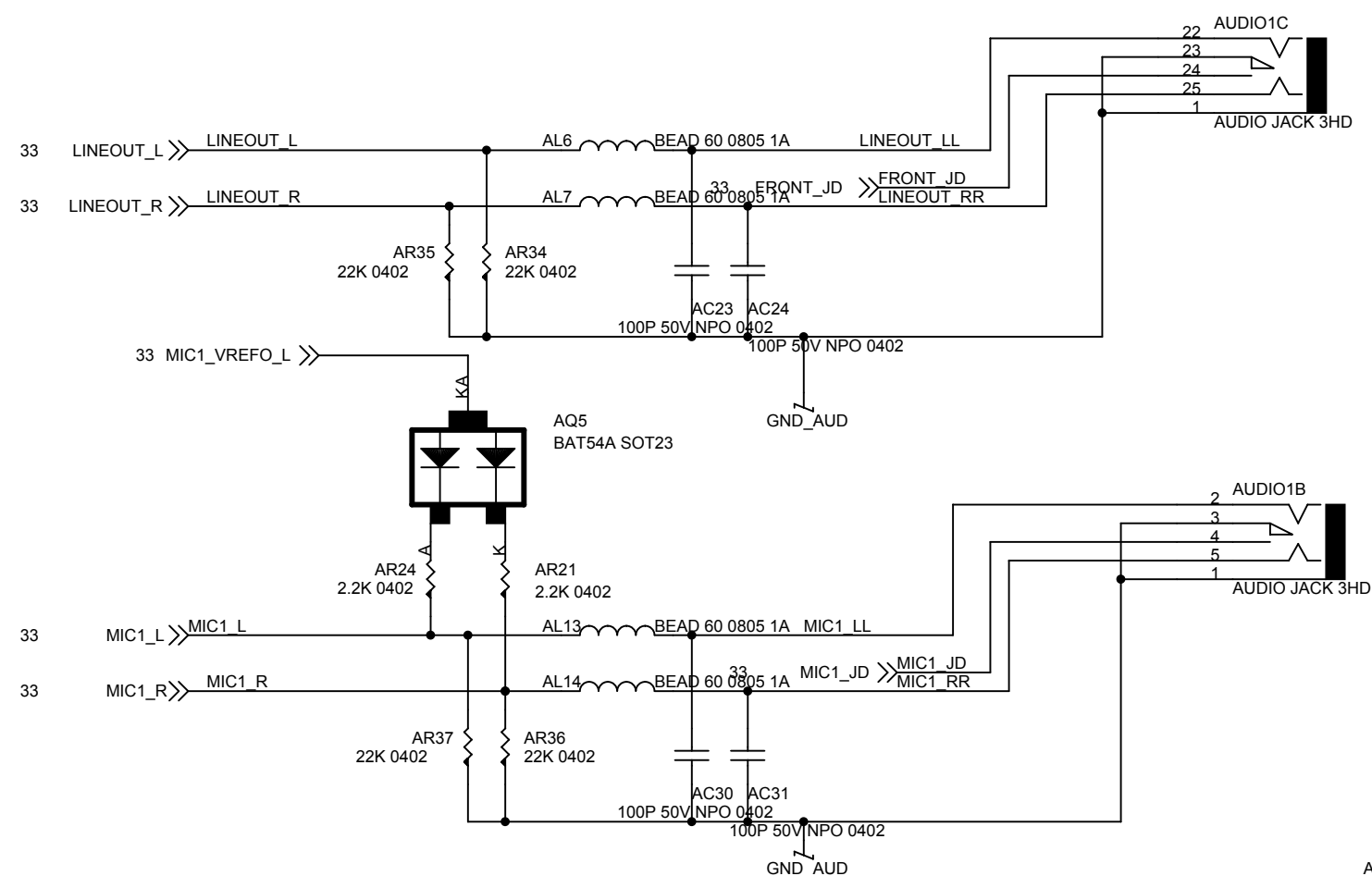
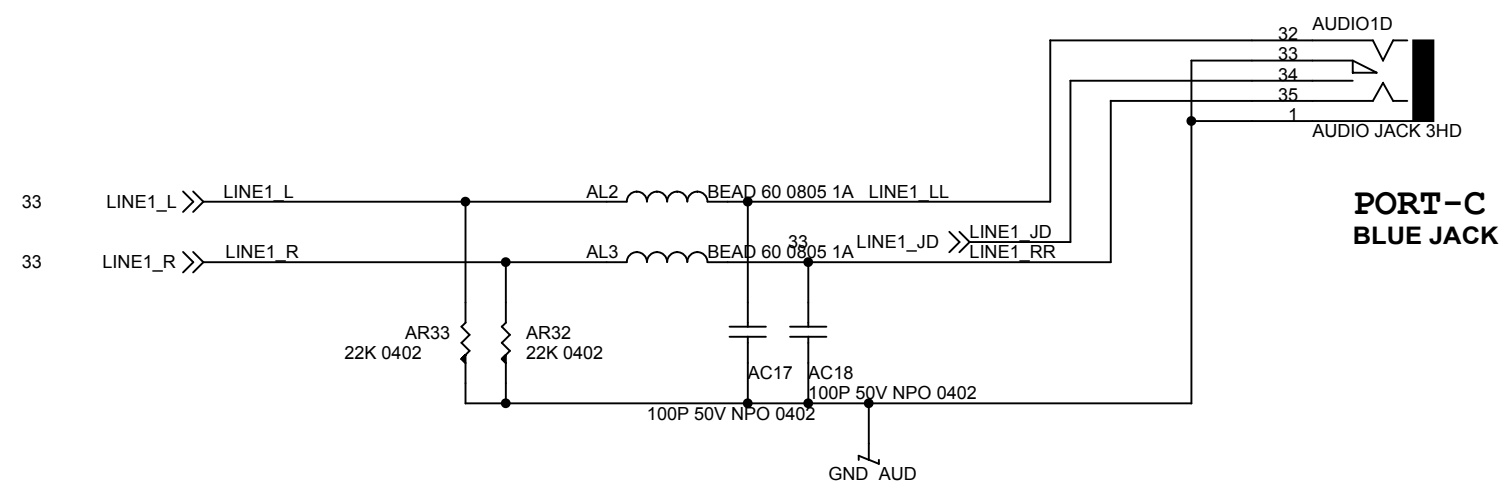
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Size	Document Number	Rev
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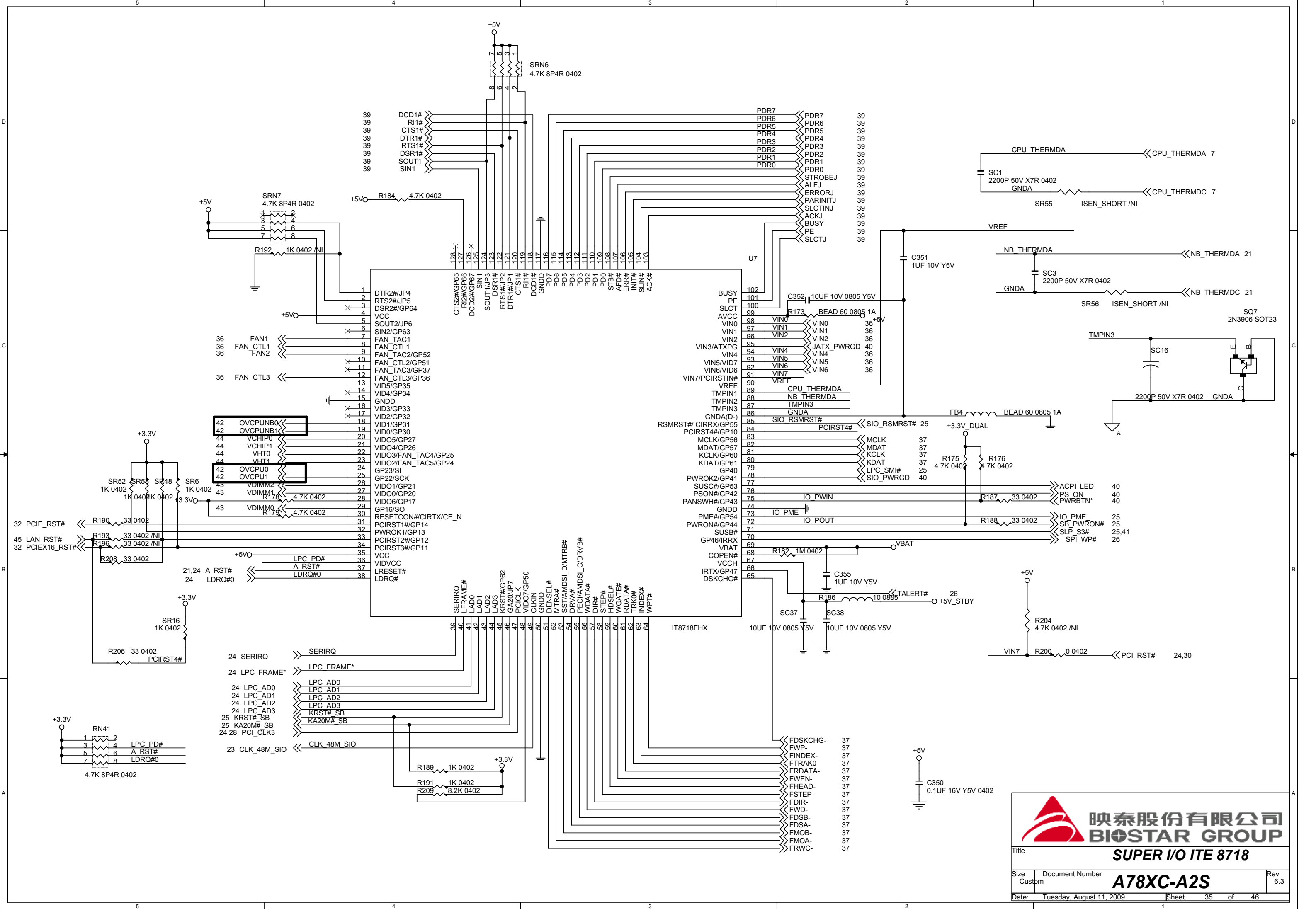
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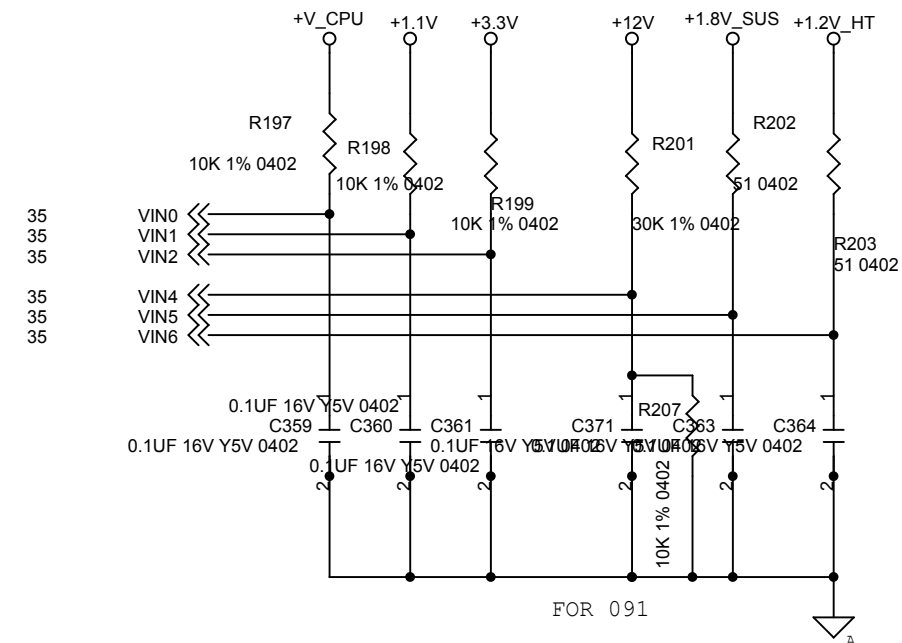
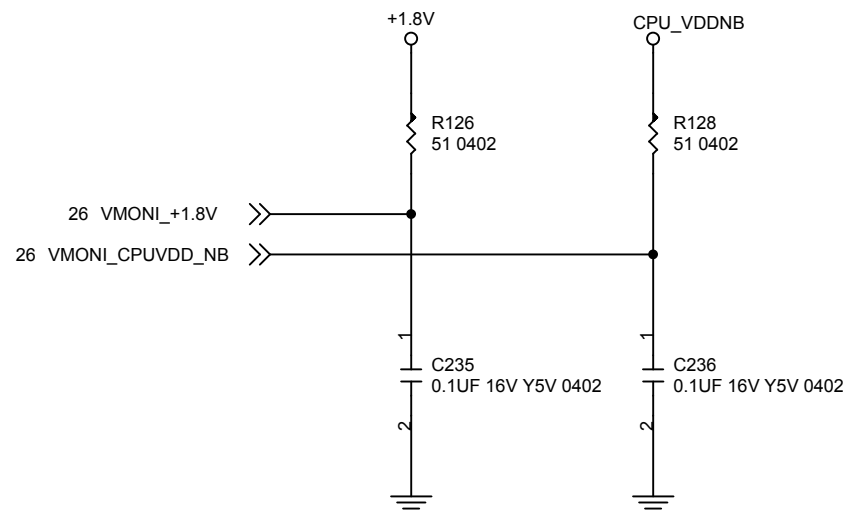




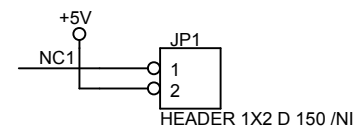
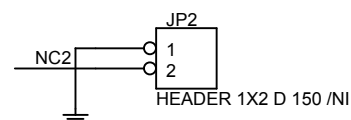
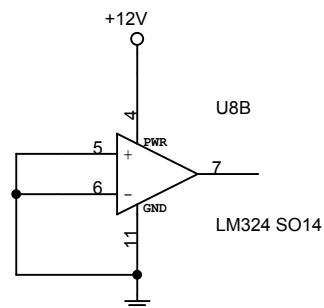
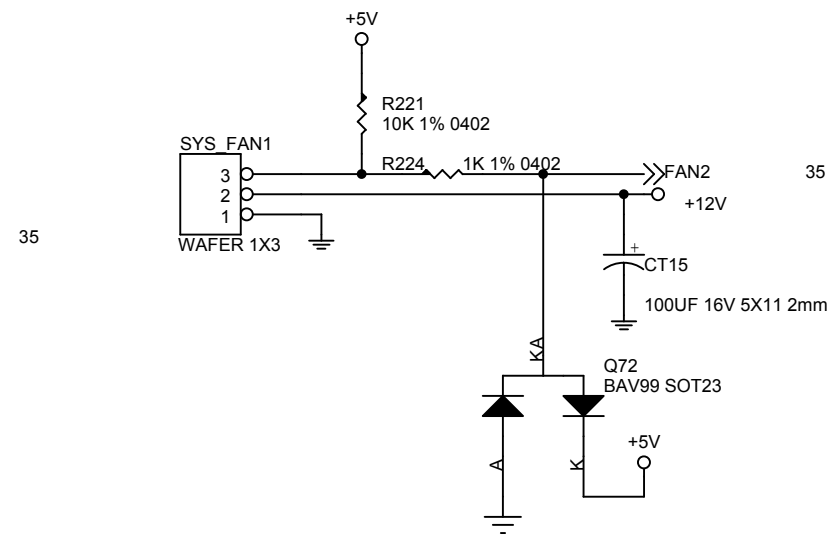
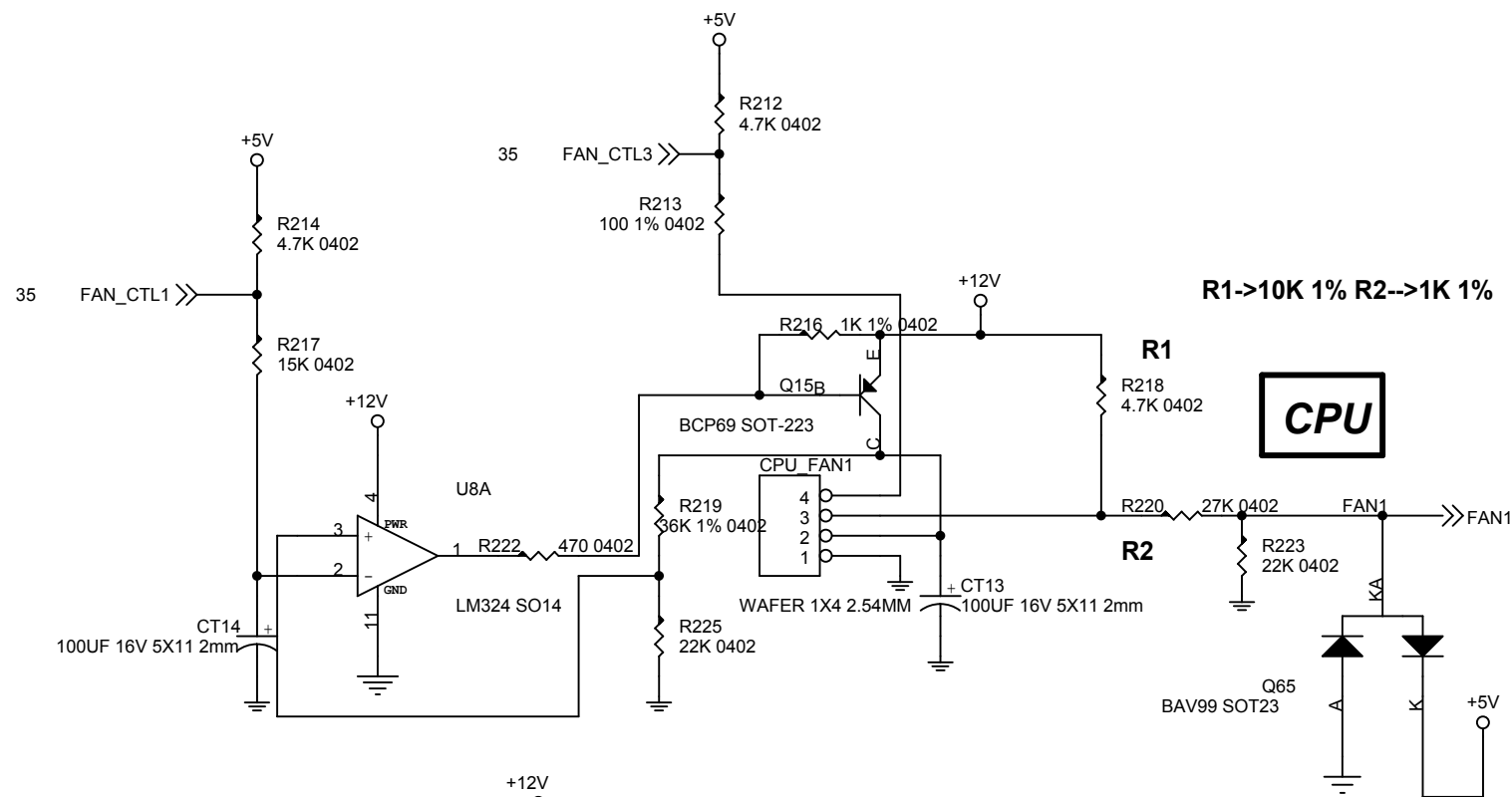




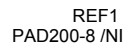


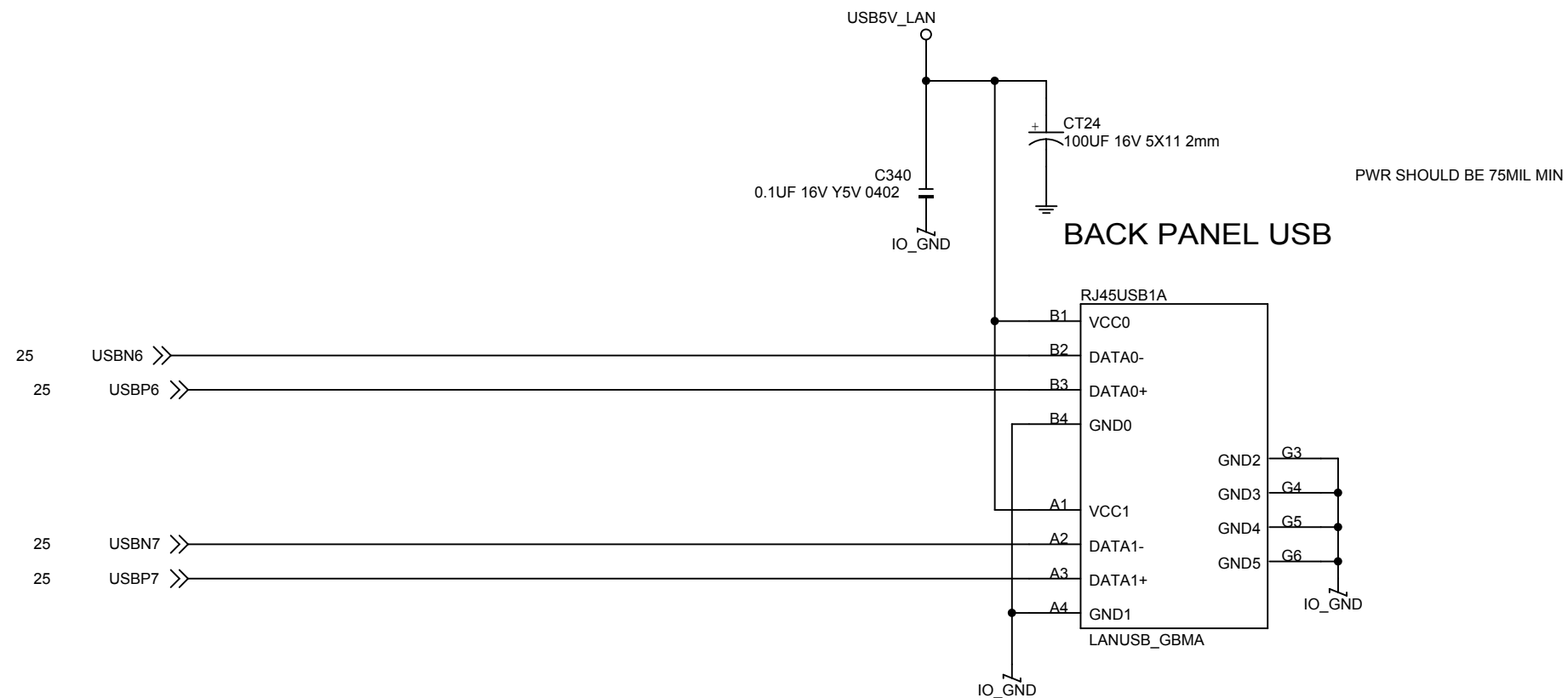


**hardware monitor**

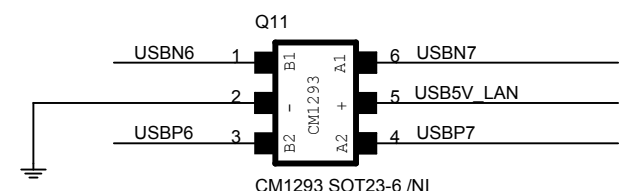




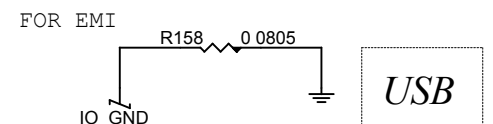
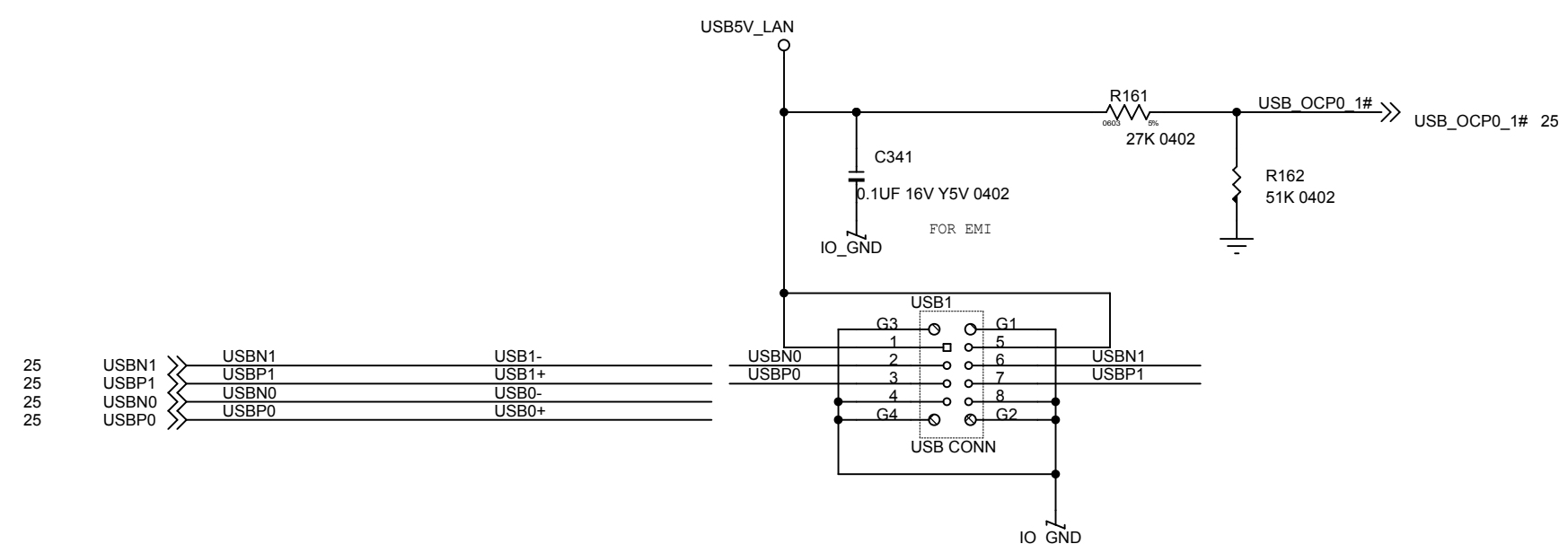
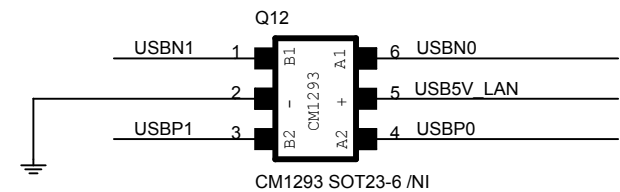




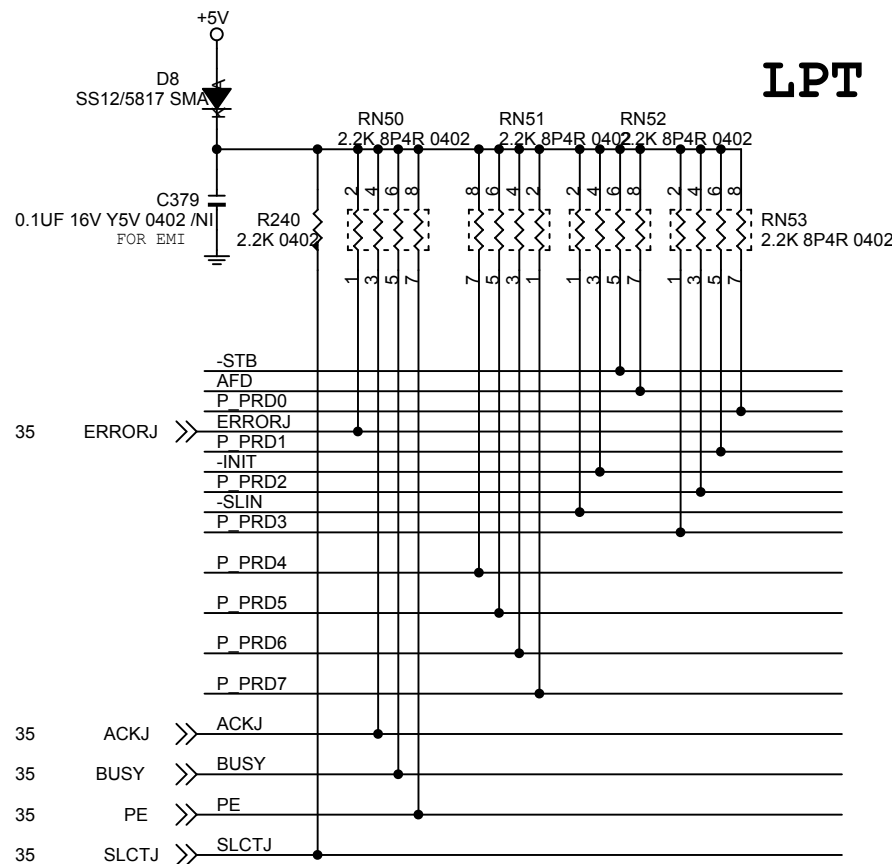
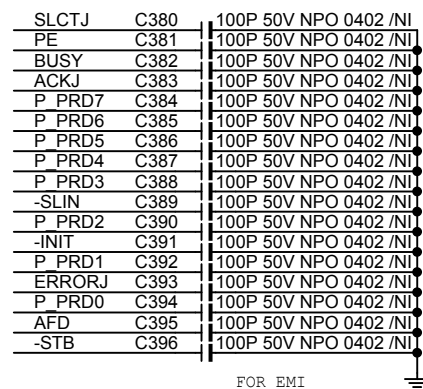
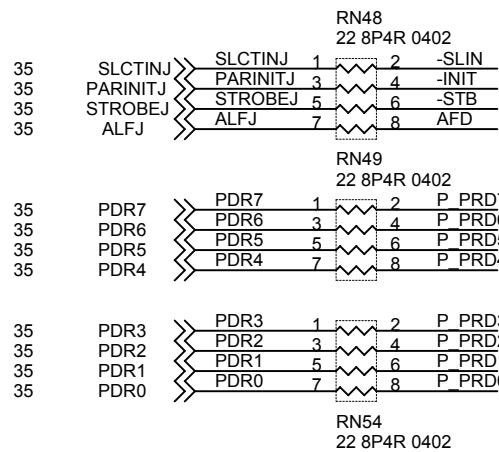
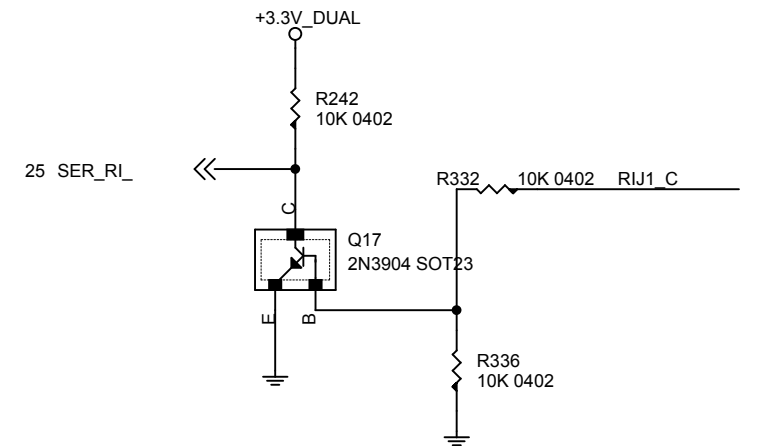
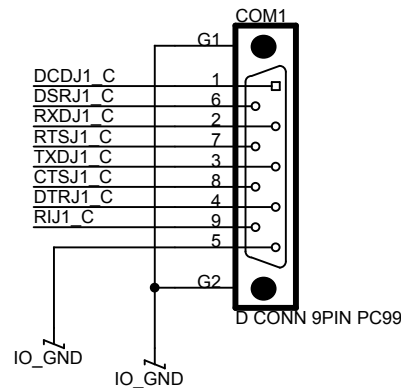
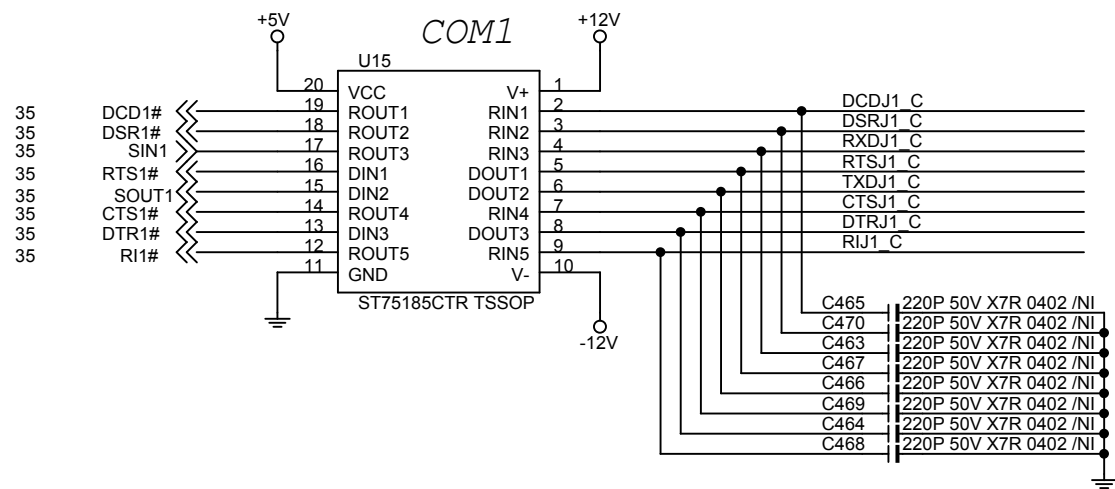
PWR SHOULD BE 75MIL MIN



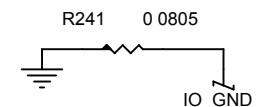
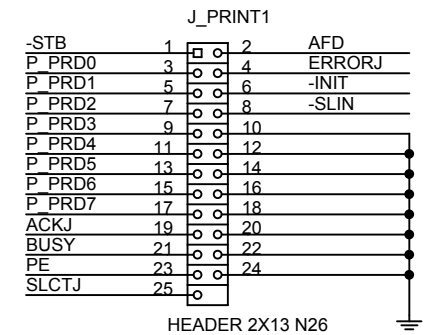
PLACE NEAR CONN




Title			<b>USB CONN</b>		
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LPT

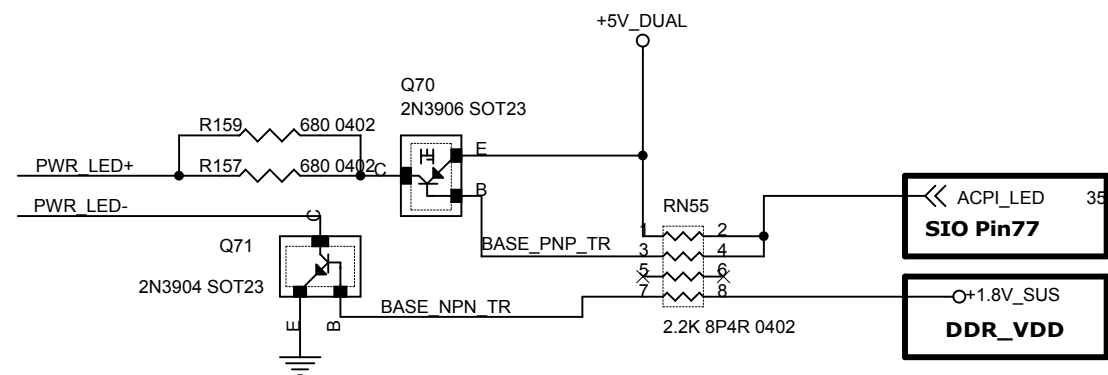
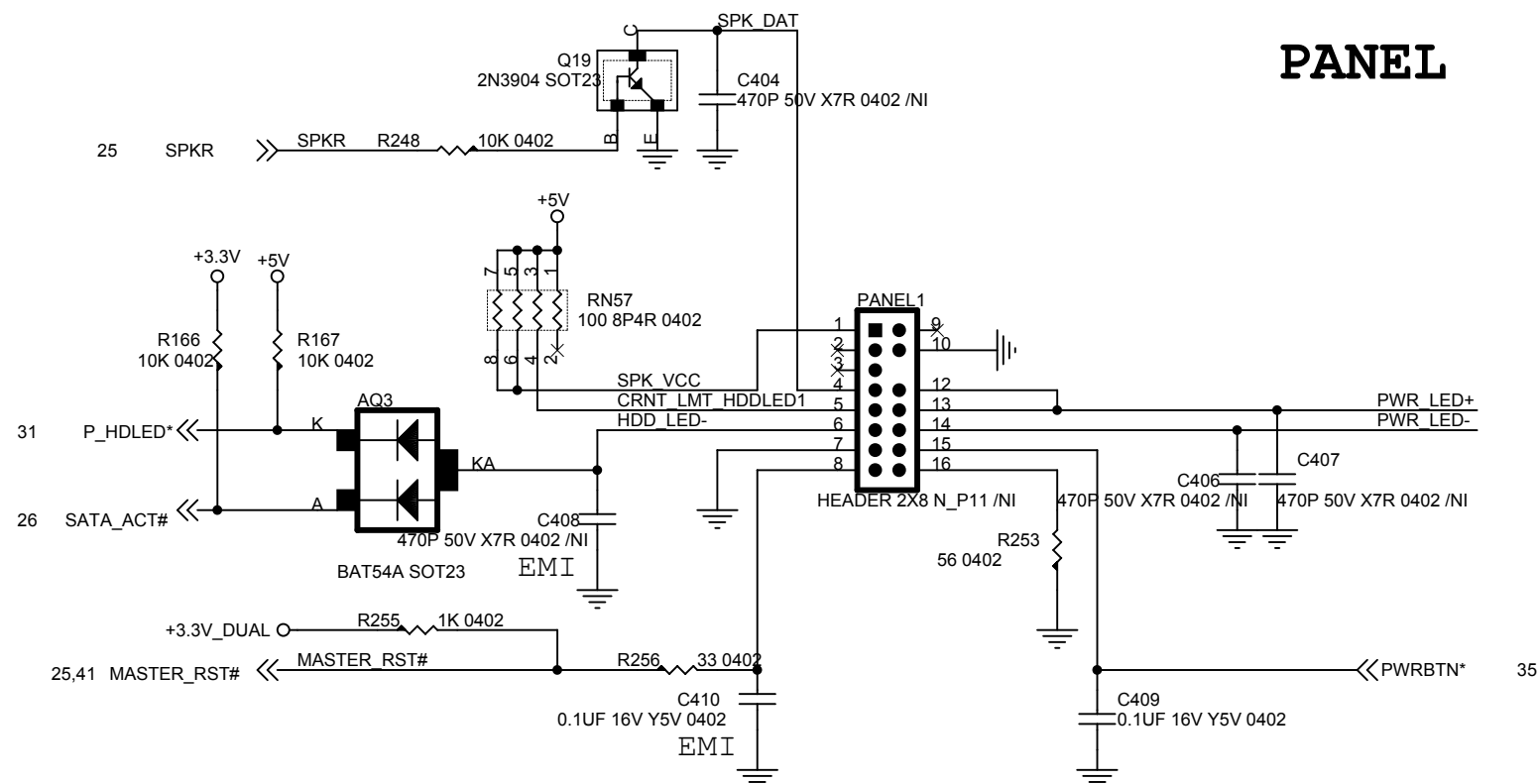
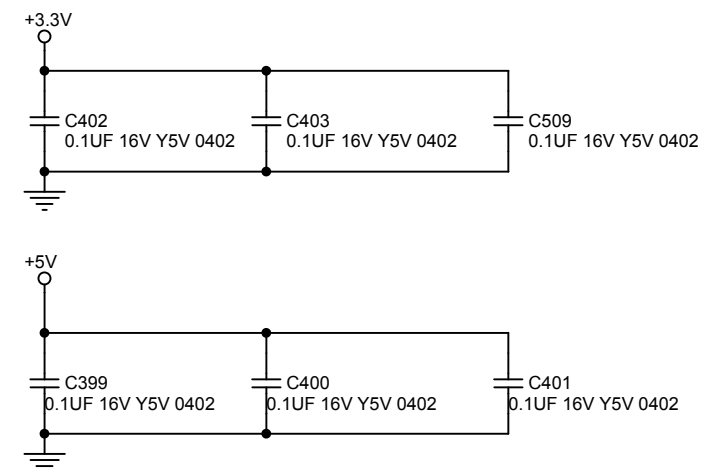
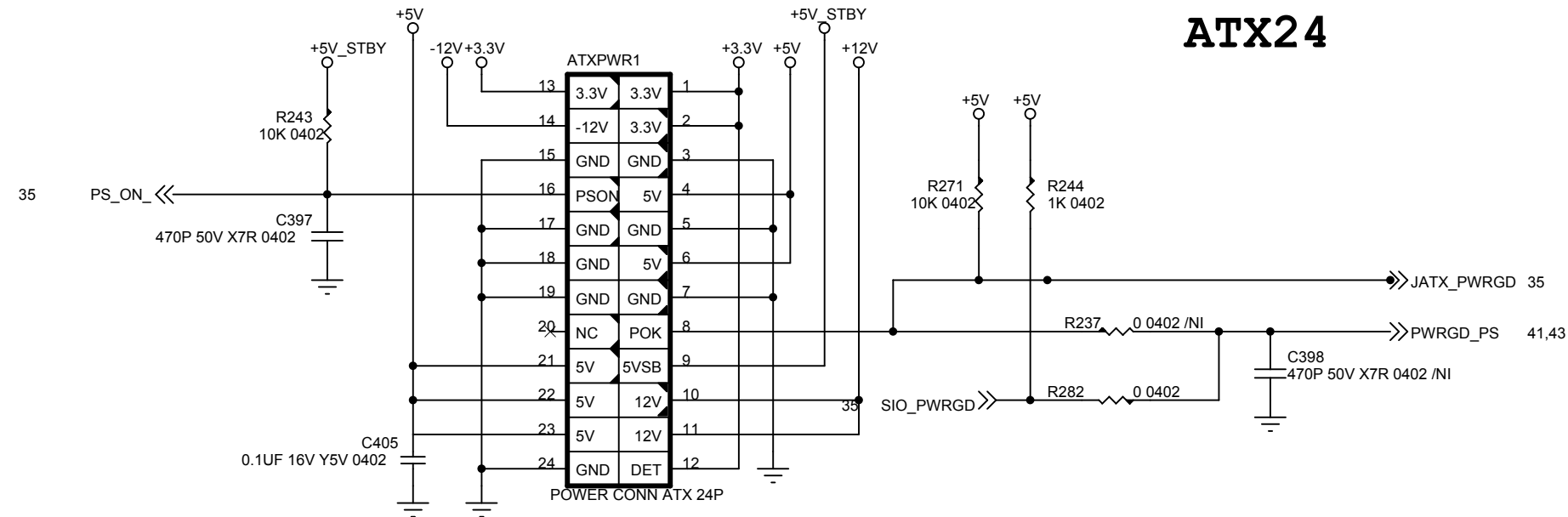


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Title **COM & PRINTER CONNECTOR**

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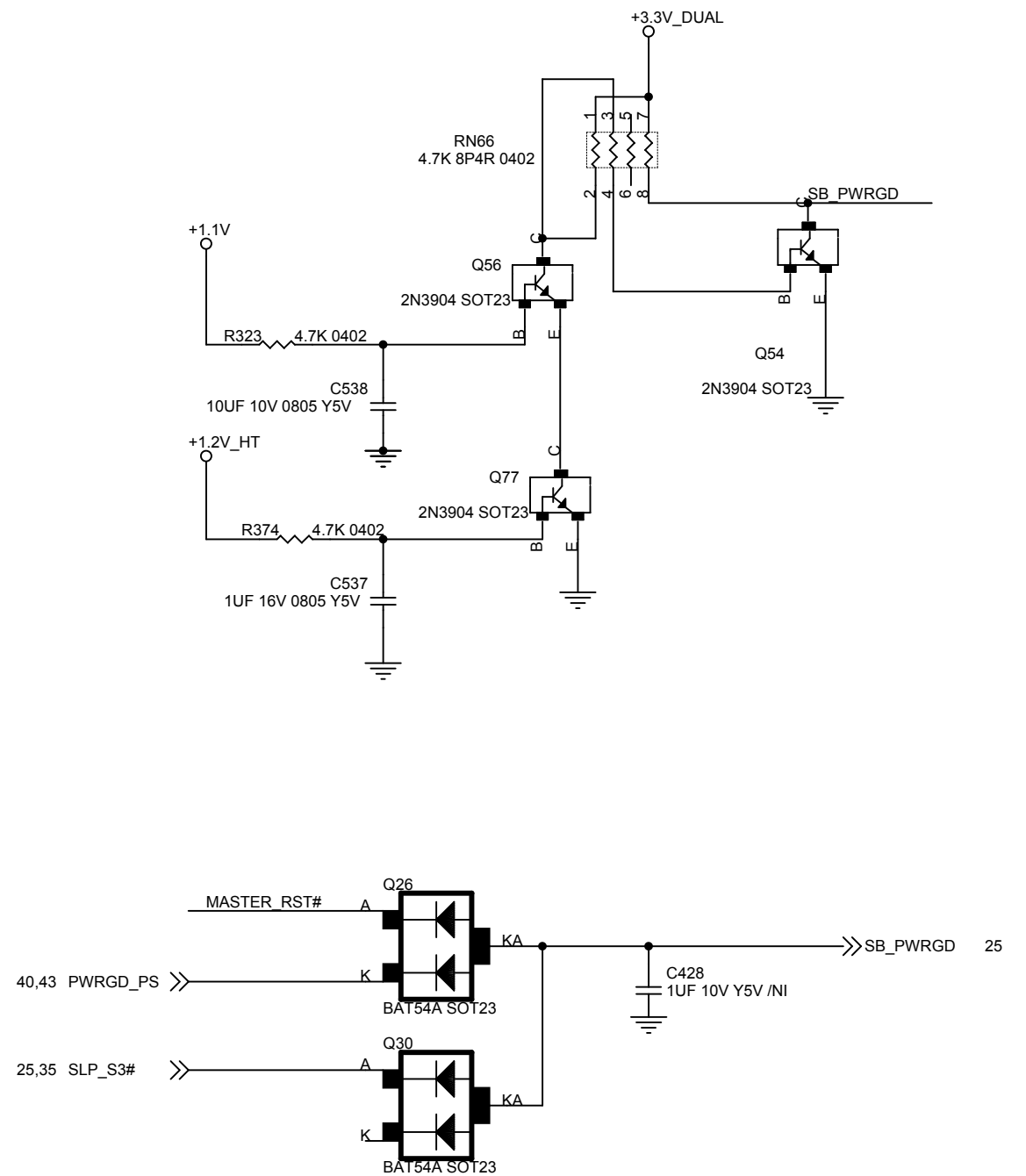
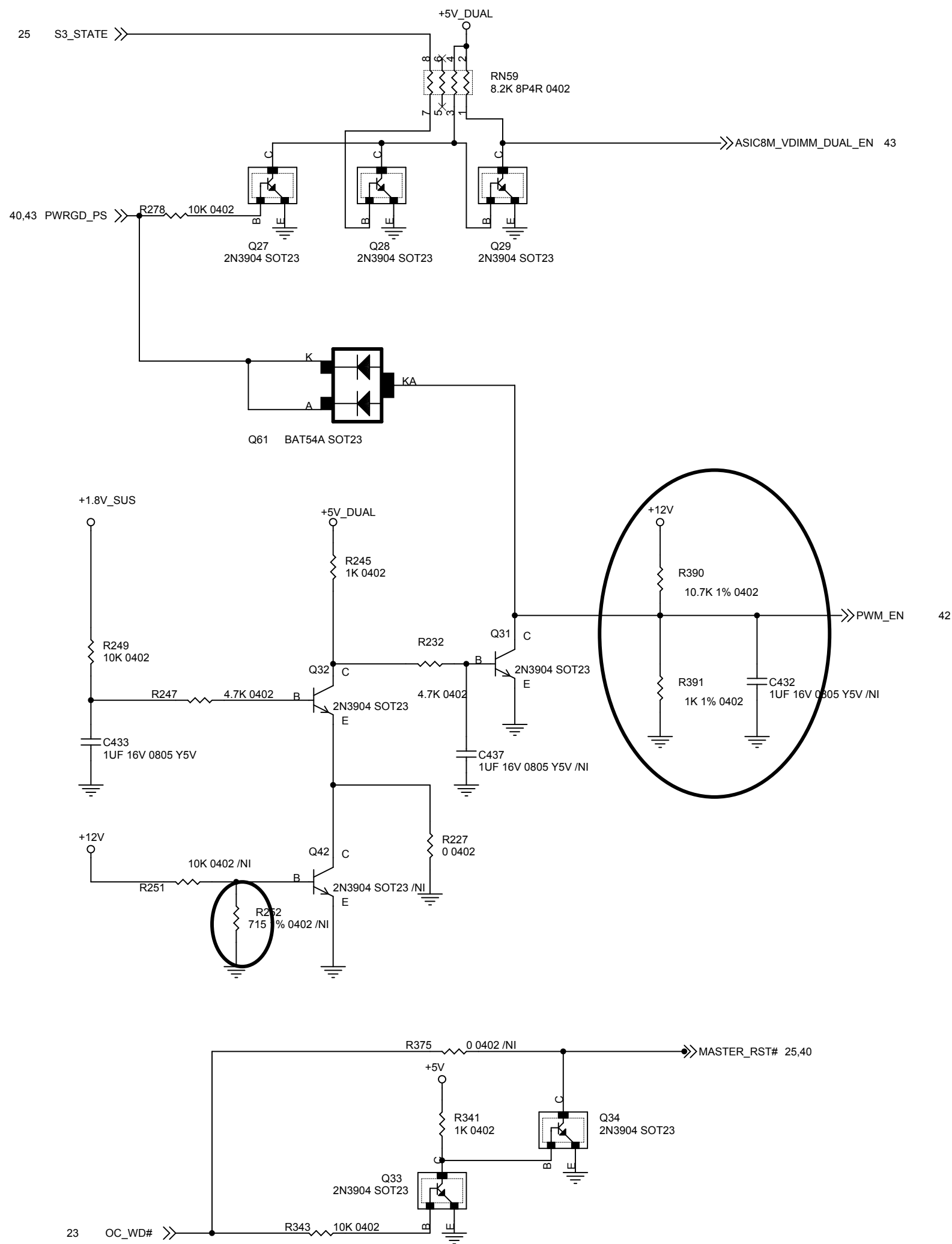


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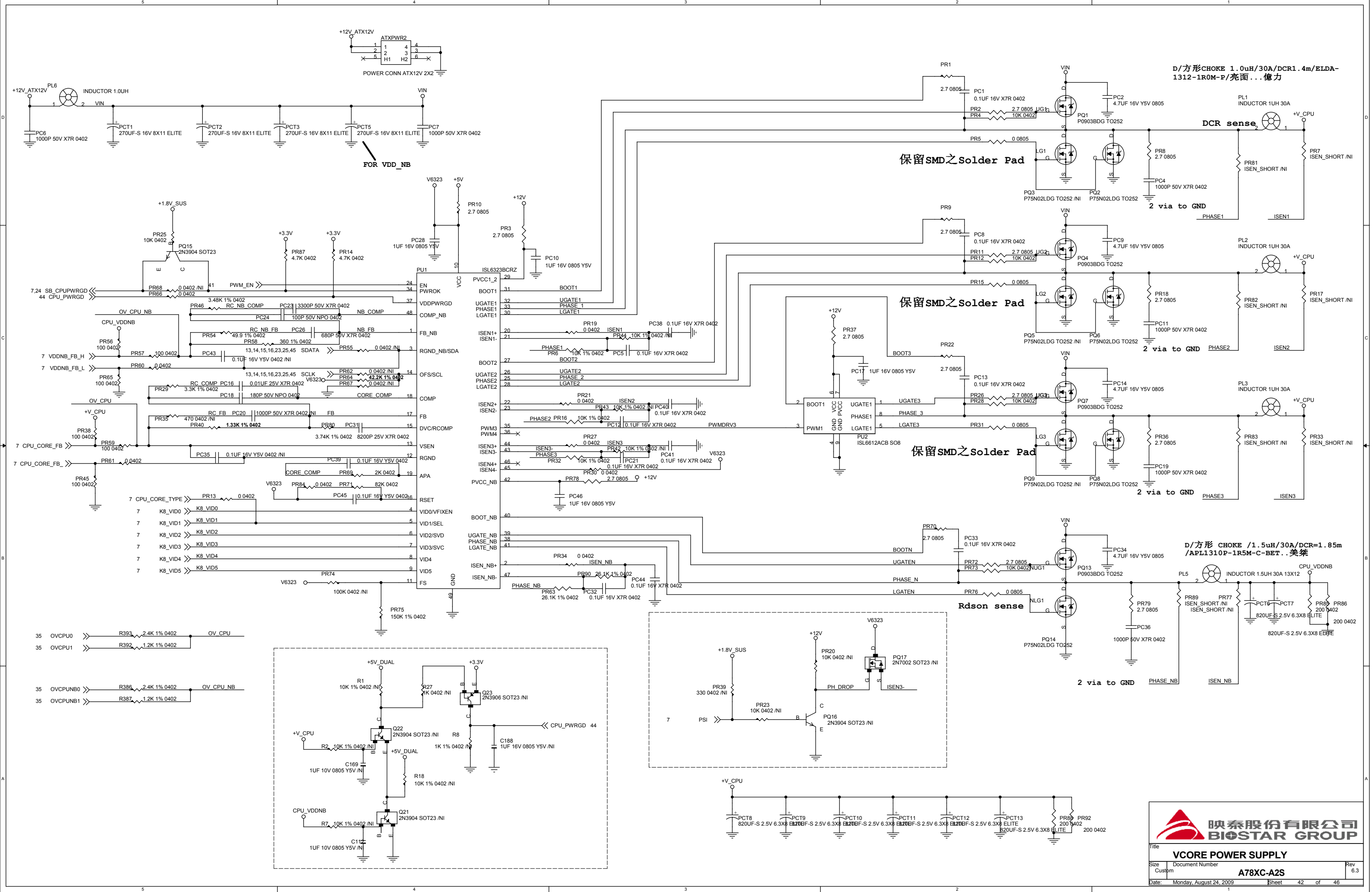
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Size Custom Document Number **A78XC-A2S** Rev 6.3

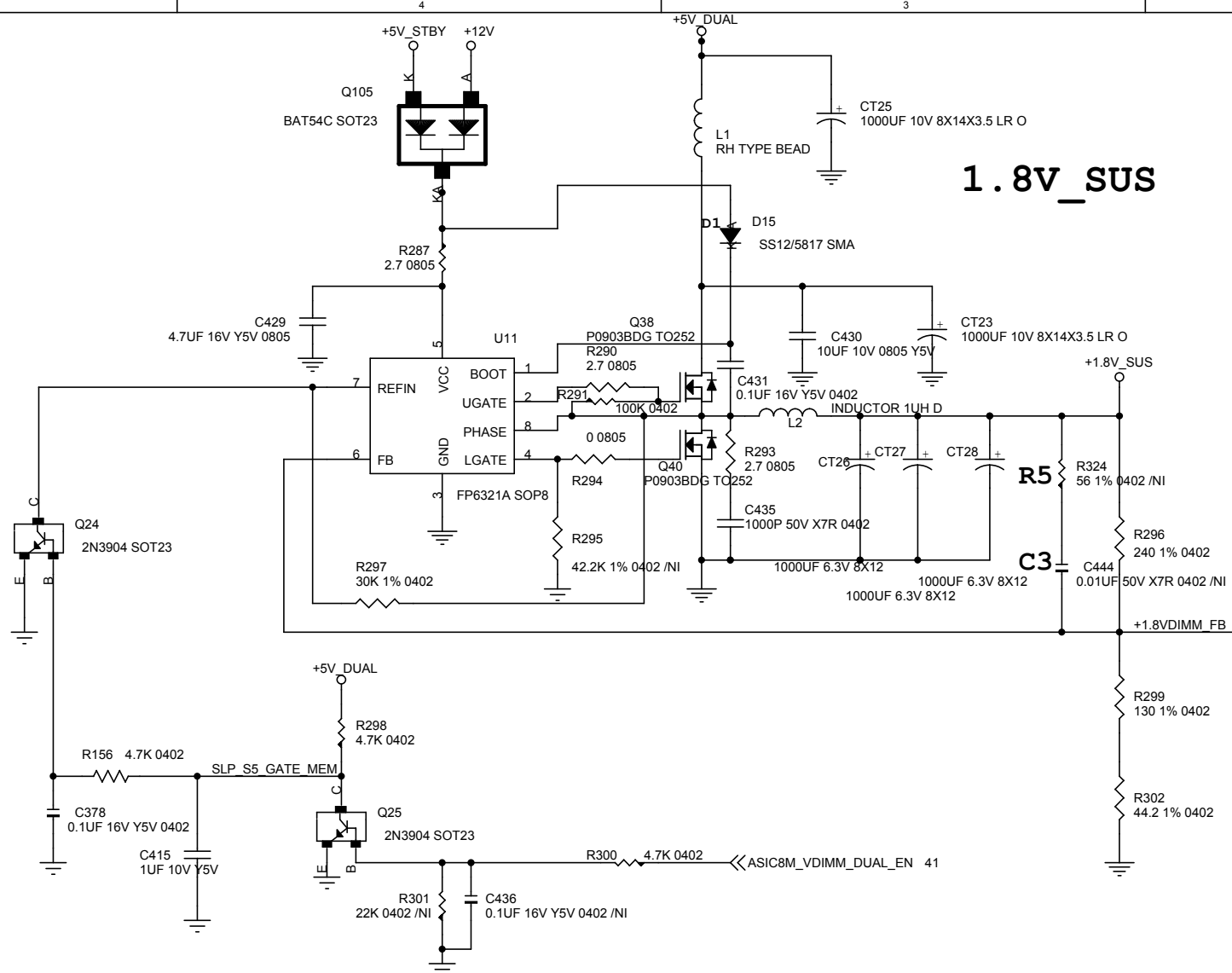
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Title			VCORE POWER SUPPLY
Size	Document Number	A78XC-A2S	
Custom			
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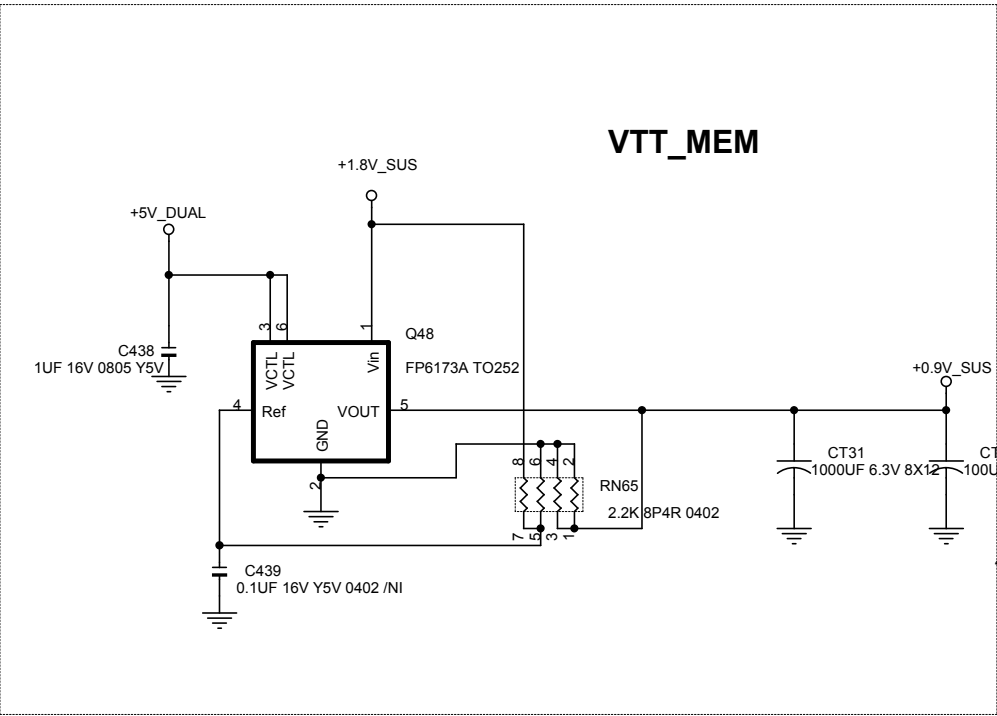


1.8V\_SUS

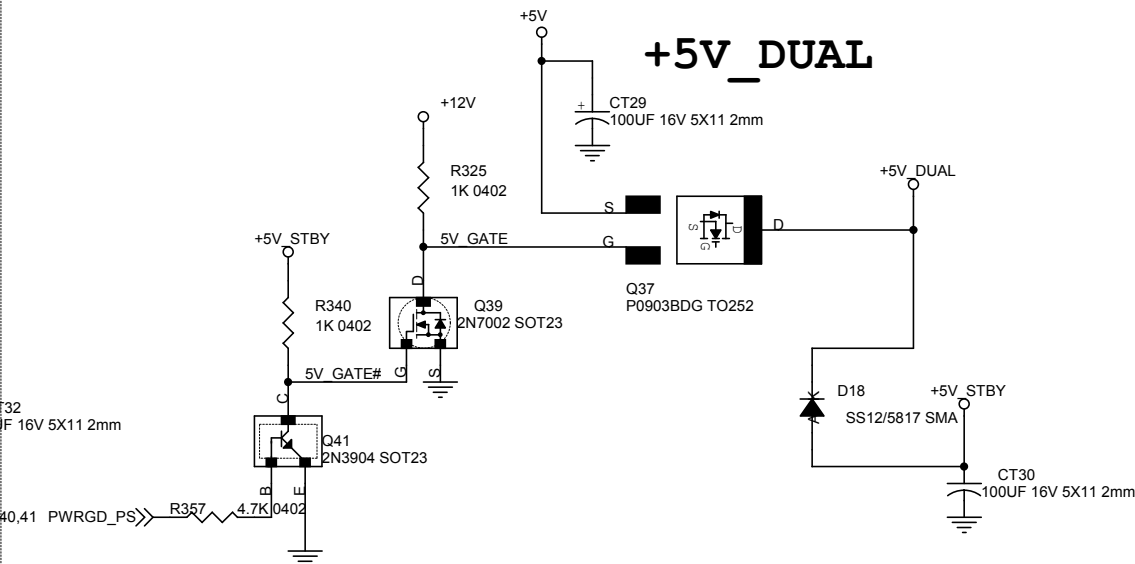
	RT9214	L6783A	UP6103
R3	NI	NI	3K 1%
R4	NI	15K	NI
R5	NI	56 1%	NI
R6	20K 1%	20K 1%	NI
C1	NI	4700P 50V X7R	NI
C2	NI	8200P 25V X7R	NI
C3	NI	0.01UF 50V X7R	NI
Vref	0.8V	0.8V	0.6V



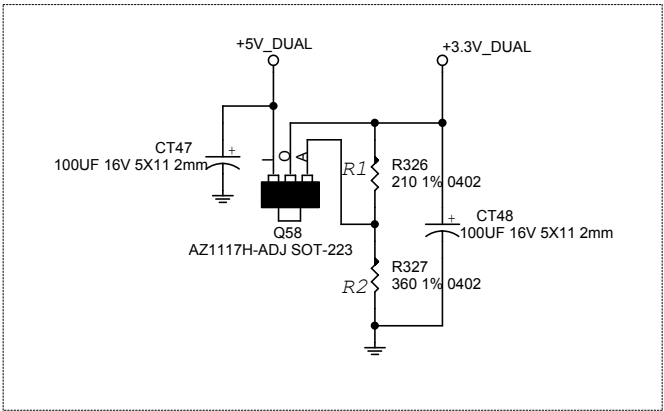
V_SM	VDIMM0	VDIMM1	VDIMM2
Default 1.90V	HR	HR	HR
1.95V	0	HR	HR
2.00V	HR	0	HR
2.05V	0	0	HR
2.10V	HR	HR	0
2.15V	0	HR	0
2.20V	HR	0	0
2.25V	0	0	0



VTT\_MEM



+5V\_DUAL



Title

MEMORY POWER

Size

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Date:

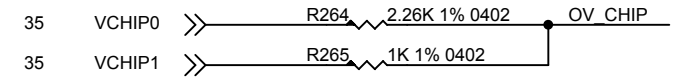
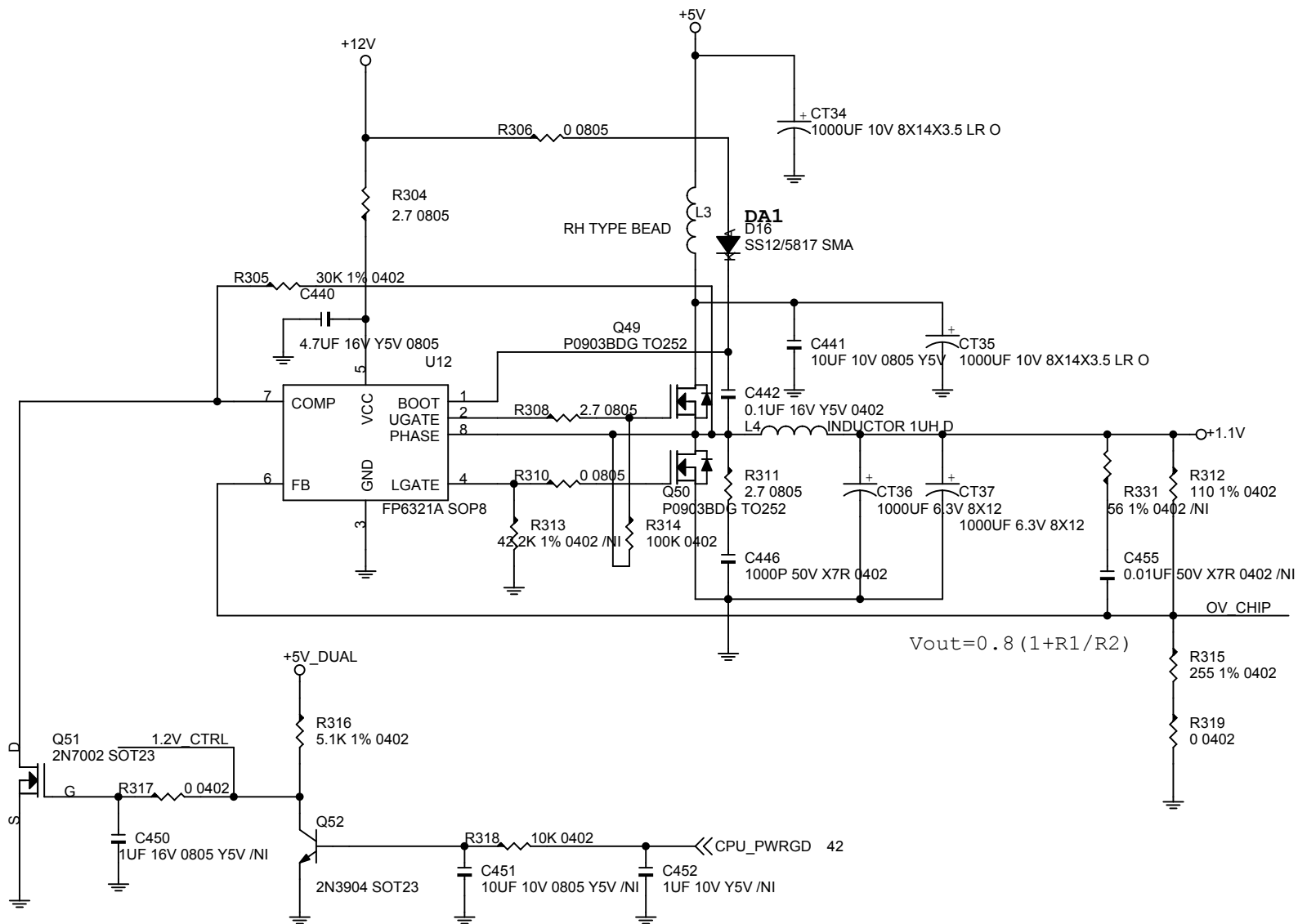
Wednesday, August 12, 2009

Sheet

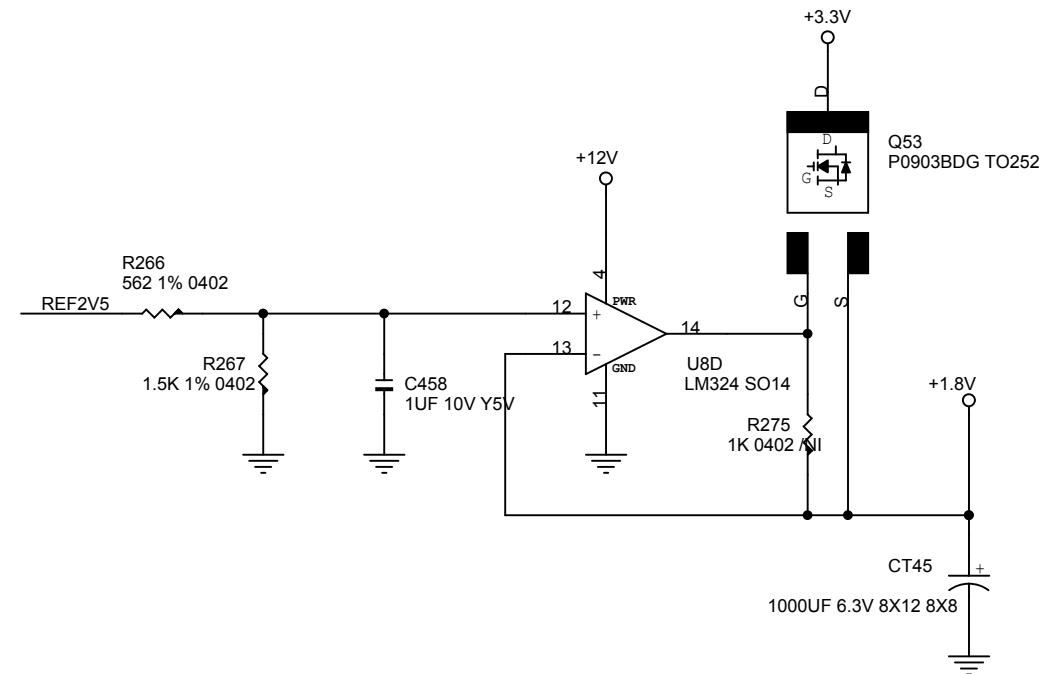
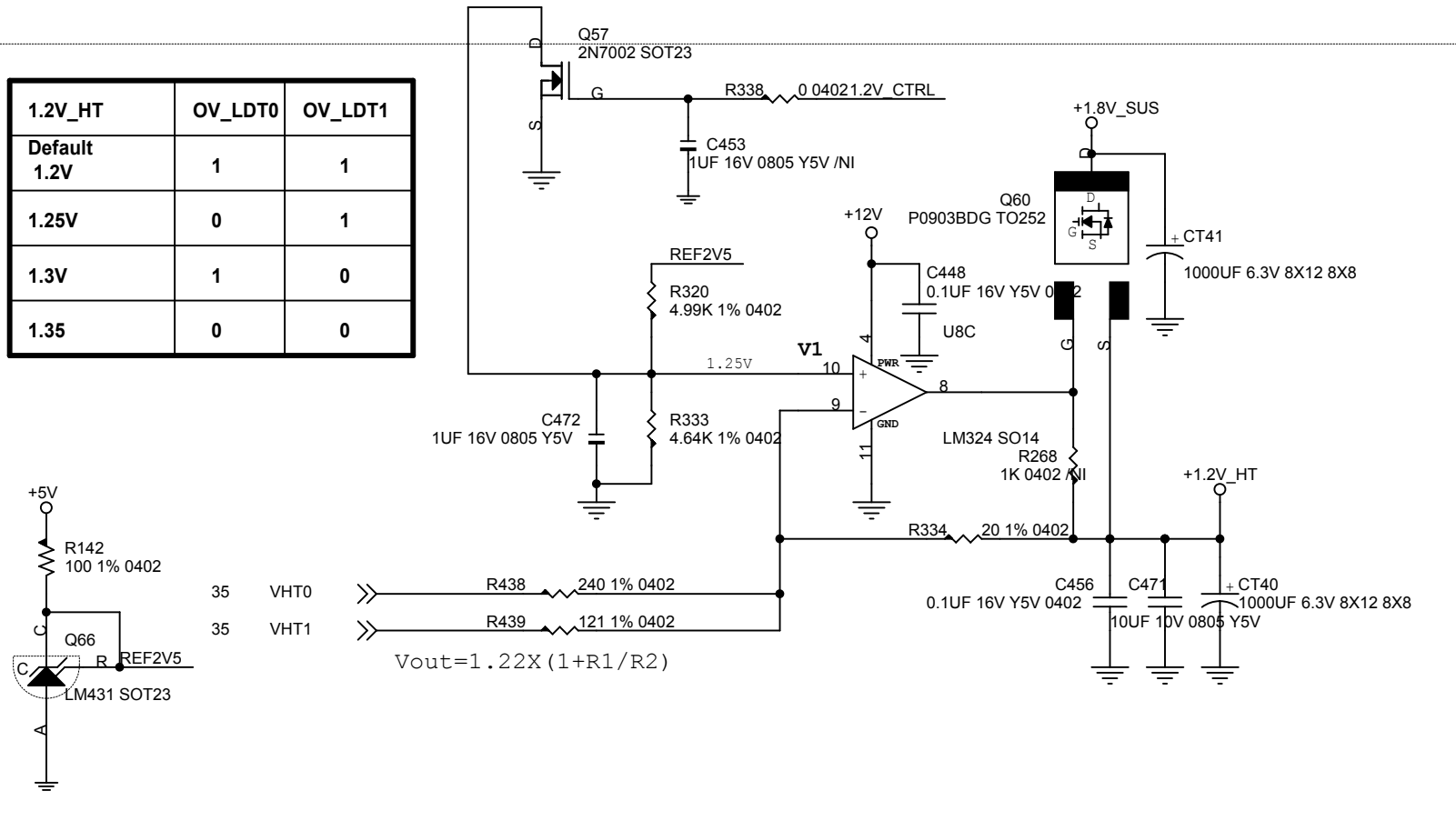
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CORE VOLTAGE	OV_CHIP1	OV_CHIP0
+1.14V(default)	1	1
+1.18V	1	0
+1.23V	0	1
+1.27V	0	0



Title

NB/SB CORE POWER

Size

Custom

Document Number

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6.3

Date:

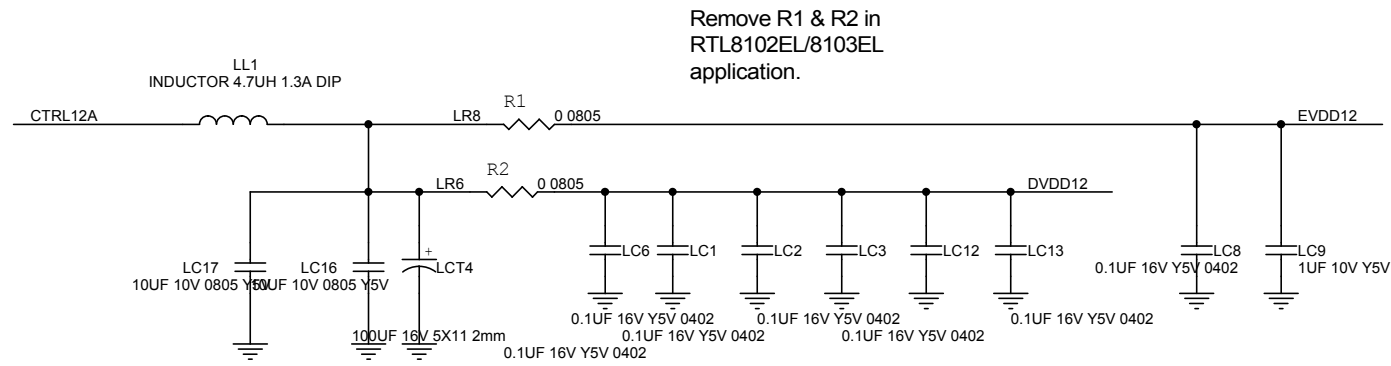
Wednesday, August 12, 2009

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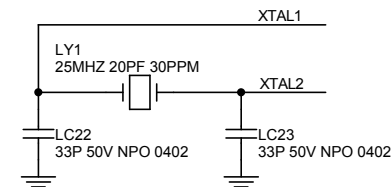
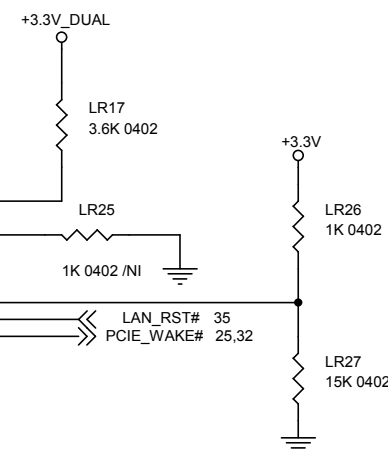
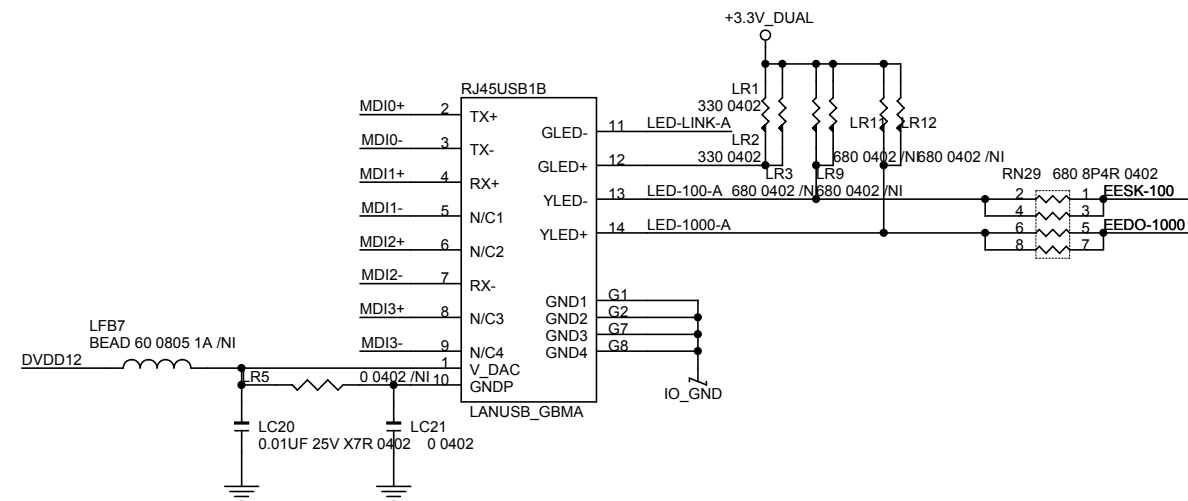
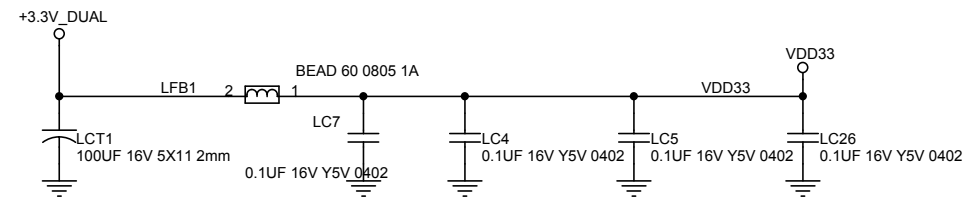
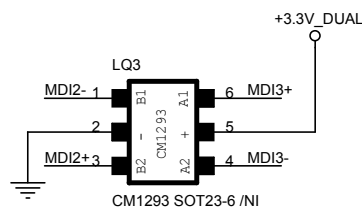
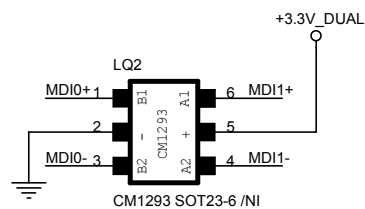
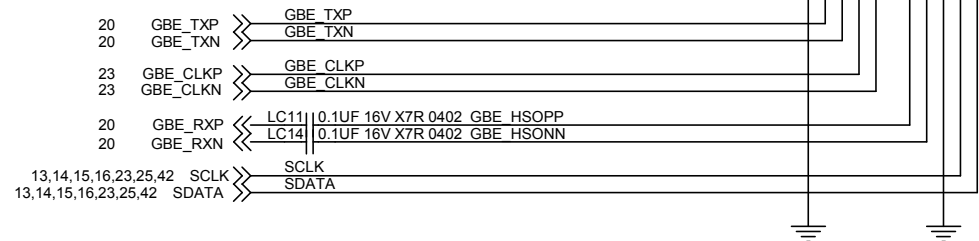
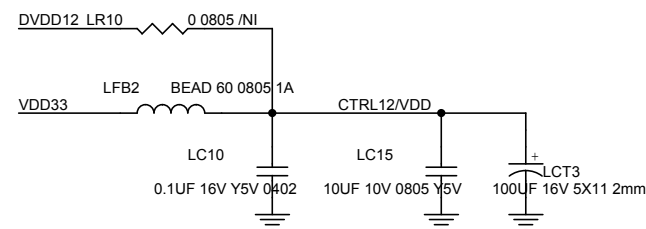
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Power domain chart	RTL8111DL
AVDD33	3.3V
DVDD12	1.05V

GbE uses Internal switching DC-DC  
10/100 uses External regulator DC-DC

For RTL8102EL, use this block.



BIOS pull high/low on Pin28  
ISOLATE to leave/enter DSM.

Remove R5 and R6 in RTL8102EL  
application.

R5 and R6 are used in the RTL8111DL application.  
Remove R6 if switching regulator is enabled.  
Remove R5 if external power 1.2V is used.

R7 value should be 2.49K (1%)  
for RTL8102EL and RTL8111DL  
application

LR25 is only required by RTL8102EL and RTL8103EL.

